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Submicrometer gate planar-doped pseudomorphic multiple-heterojunction MODFETs for millimeter-wave and optical communication

Chen, Young-Kai, Ph.D.

Cornell University, 1988

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SUBMICROMETER GATE PLANAR-DOPED PSEUDOMORPHIC MULTIPLE-HETEROJUNCTION MODFETS FOR MILLIMETER-WAVE AND OPTICAL COMMUNICATION

A Thesis

Presented to the Faculty of the Graduate School

of Cornell University

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

Young-Kai Chen

May 1988

BIOGRAPHICAL SCETCH

Young-Kai Chen was born in Taipei, Taiwan on October 7, 1953. He received the B.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan in 1976. From 1976 to 1978, he served in the Chinese Air Force as an instructor in the Air Force Electronic Communication School. From 1978, he attended Syracuse University, and received the M.S. degree in Electrical Engineering in 1980. For his master's thesis, he worked on the synthesis of an optimal two-dimensional phase array antenna under the supervision of Professor David K. Cheng. Since 1980, he has been with the Electronics Laboratory of General Electric Company, Syracuse, New York, working on the modeling, design and testing of high speed silicon and GaAs integrated circuits.

He attended the School of Electrical Engineering at Cornell University in 1985. He has been working on compound semiconductor devices and their circuit applications for his thesis research. Dr. Chen is the author of several papers and holds two U.S. patents in the areas of GaAs integrated circuits.

To

my parents, my wife Carol and

my children Jennifer and David

for their love and supports

throughout this thesis

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CHAPTER 1

INTRODUCTION

1.1. Review of Historical Developments

Esaki and Tsu first suggested the concept of utilizing a modulation doping technique to spatially separate electrons from their ionized parent donors at an abrupt heterojunction interface [1]. Electrons from donors in the wider bandgap materials are confined in a two-dimensional potential well in the narrower bandgap material forming a Two-Dimensional Electronic Gas (2DEG). The separation of these electrons from the ionized donors results in high electron concentration without being penalized by imputity scattering. Enhanced electronic transport properties such as higher low-field mobility and saturation velocity should be the results for transport parallel to the heterointerface. The quantized energy level in the potential well in the direction perpendicular to the heterointerface has also been a very interesting subject to many solid-state researches to study behaviors of quasi-two-dimensional systems [2]. With the advancement of Molecular Beam Epitaxy (MBE) technology, this concept was demonstrated by Stormer et al. on the $Al_xGa_{1-x}As$/GaAs material system [3]. Subsequently, much attention has been focused on the modulation-doped structures in order to realize very high speed active devices. In 1980, the first functional field-effect transistor using this technique was reported [4].

Among many combinations of compound semiconductor heterojunction structures, most of the research and development works of MODFETs have been performed on the lattice-matched AlGaAs/GaAs material system to utilize the intrinsic high low-field mobility of the narrow bandgap GaAs channel and to minimize potential defect densities at the heterojunction interface. An important consideration in selecting a heterojunction structure is the conduction band discontinuity (ΔE_C) at the heterointerface. Small conduction band discontinuity results in less electron transfer across the heterojunction to form the 2DEG. The small discontinuity also leads to inefficient charge control in the MODFET structure from a parasitic MESFET effect [5] and an insufficient barrier height to reduce hot electron effects [6]. Recently, a new type of MODFET based on the lattice-strained or pseudomorphic quantum-well structure has attracted a lot of attention [7]. Improved microwave performance has been obtained with AlGaAs/InGaAs/GaAs pseudomorphic MODFETs by incorporation of indium in the thin quantum-well channel to have higher electron velocity and larger conduction band discontinuity [8] with the lattice-mismatch accommodated by the lattice strain [9]. To the extreme of epitaxial growth on the lattice-matched or lattice-strained substrates, MODFETs grown on lattice-mismatched substrates have been reported with very good microwave performance [10],[11].

The maximum obtainable value of the sheet charge density of 2DEG is limited by the material parameters of single heterojunction MODFETs such as the

thickness of spacer layer, conduction band discontinuity, etc. It is generally considered difficult to generate a 2DEG density more than $1x10^{12}\ cm^{-2}$ in the AlGaAs/GaAs system. Although these material parameters may be improved by using a different material system, an alternative approach is to utilize multiple heterojunction modulation-doped structures to increase the total charge density [12].

The high silicon doping density in the conventional uniformly-doped AlGaAs layer leads to low gate breakdown voltages, device instability at low-temperature [13], and process control problems such as maintaining threshold voltage uniformity. Planar-doping techniques were developed to introduce silicon donors within a few atomic planes of a GaAs layer during an MBE growth interruption [14]. DH-MODFETs with atomic planar-doped AlGaAs layers show little light sensitivity at low temperature as well as improved breakdown voltage and power-added efficiency [15].

With advancements in the fine-line lithography to define submicrometer gate dimensions and epitaxial technology to form abrupt heterojunctions, very rapid progress has been made in establishing the Modulation-Doped Field-Effect Transistor (MODFET) as a key active device for high frequency analog and digital applications. Very short propagation delay of 5.8 ps at 77 K [16] and 7.2 ps at 300 K [17] has been demonstrated with digital ring oscillator circuits. In the area of analog applications, a very low noise figure of 2.3 dB was

achieved at 59 GHz [18] and a high power density of 1 W/mm was obtained at 21 GHz [19]. A very large current density of 1100 mA/mm has also been achieved with decent microwave performance from a multiple quantum-well MODFET [20]. Because of the good optical properties of direct-bandgap GaAs material system, the capability of direct detection of high speed optical signals has also been demonstrated with modulation-doped heterostructures [21], and MODFETs are very promising to build a new semiconductor technology for high speed optical communication and computation systems.

1.2. Thesis Outline

The scope of this thesis is to investigate the characteristics of MODFETs with double and multiple heterojunctions for high speed large-signal applications where both large current density and high power gain cut-off frequency are needed.

The charge control model is very important to understand the operation of MODFET, and it also serves as the physical basis of a computer simulation program to analyze the device current-voltage characteristics and to further predict the performance of MODFET circuits. Chapter 2 describes charge control models of MODFETs with either single or double planar-doped AlGaAs layers together with the analysis of some figures-of-merit.

The non-linear small-signal AC parameters are very important to study the dynamic properties of FETs and to establish the data base for modeling the

large-signal device behaviors [22]. The bias-dependence of the equivalent circuit parameters was studied at 4 GHz for a single heterojunction MODFET [23] and over a broad frequency range for a double heterojunction MODFET [24]. Because the high frequency figures-of-merit are directly related to the equivalent circuit parameters, this study provides rich information between the RF performance and device design parameters of DH-MODFETs. Chapter 3 studies the bias-dependence of the equivalent circuit parameters of a DH-MODFET with measured broadband microwave scattering parameters. The equivalent circuit parameters and high frequency gains are influenced by the distinctive features of MODFETs, such as heterojunction charge control, AlGaAs parallel conduction, and real-space transfer.

Parasitic conduction current in the buffer layer increases the output conductance and severely limits the operation frequency range of multiple heterojunction structures. Low doping densities along with tight charge control at the bottom inverted heterointerface are needed to reduce the substrate current. High electron-barrier buffer layers such as AlGaAs/GaAs superlattices and buried p^+-GaAs layers have been suggested to improve the charge control and hot carrier confinement at the bottom heterointerface in DH-MODFET structures [25].

Chapter 4 studies the effect of buffer layer structure on the microwave characteristics of pseudomorphic GaAs/InGaAs/AlGaAs DH-MODFETs.

Reduced sub-threshold current, improved output conductance, and enhanced two-dimensional electron carrier confinement are obtained from the fabricated MODFETs with either 1.2-μm or 0.3-μm gate length. As a result of the different buffer structures, an f_{MAG} up to 200 GHz is obtained from a 0.3-μm DH-MODFET with a superlattice buffer layer, and a full channel current of 720 mA/mm is demonstrated by a 0.3-μm DH-MODFET with a superlattice buffer layer. CW power density up to 0.6 W/mm is obtained at 18 GHz with good efficiency and linear gain. Detailed studies show the significance of carrier de-confinement caused by real-space transfer of the hot two-dimensional electrons on the performance of short-channel MODFETs.

By effectively suppressing the positive output conductance generated by the substrate-bound hot electrons with high potential barrier buffer layers, real-space transfer of hot electrons into the top electron supplying layer could be observed in the MODFET structures [26]. Chapter 5 examines mechanisms of generating the DC negative differential resistance at high gate bias voltages. A tuned microwave oscillator, based on the real-space transfer negative resistance, is also realized with a fundamental oscillation frequency up to 19.68 GHz at room temperature.

Photoconductive detectors fabricated on the modulation-doped heterojunction structure have demonstrated very fast response to picosecond light pulses, and is very promising for the Opto-Electronic Integrated Circuit (OEIC) technol-

ogy [21]. Chapter 6 examines the optical response of different DH-MODFET structures for the detection of picosecond laser pulses. Optical gain up to 1,800%, fast risetime of 1.6 ps, and broad bandwidth up to 10 GHz can be obtained utilizing various layer structures. Buffer quality, hot electron dynamics, and device RC parasitics are found to be the limiting factors.

Chapter 7 investigates a different category of the MODFET structure, that is the dual-gate MODFET. By using the dual-gate topology, the performance of the single gate MODFET, such as the gain and stability, can be enhanced significantly without modifying the processing steps and layer structures [27]. Different gain roll-off slopes are observed over a broad measurement frequency, and will be analyzed by the equivalent circuit model.

The results of this thesis are summarized in Chapter 8, and some suggestions for the future work is proposed.

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CHAPTER 2

CHARGE CONTROL MODEL

2.1. Introduction

The Modulation-Doped Field-Effect Transistor (MODFET) is a very promising candidate for both microwave, millimeter-wave, and digital circuits [1]. In order to achieve high sheet charge density in the two-dimensional channel and to maintain a high gate-to-channel aspect ratio for high frequency applications [2], most of the conventional MODFET structures employ highly-doped AlGaAs electron supply layers. This leads to problems such as low breakdown voltage, low activation efficiency of dopants, low-temperature instability and light sensitivity [3]. In 1979, Wood [4] reported a GaAs power MESFET structure of which the dopants were deposited on one atomic plane by interrupting MBE growth. This atomic doping technique was used to synthesize complex free-carrier doping profiles. Lee [5] introduced this technique to place the silicon doping in the AlGaAs layer and demonstrated a spread of silicon atoms as small as 100A. Improved gate-to-drain breakdown voltage up to 19 volts and much reduced low-temperature (77K) light sensitivity were demonstrated in a double heterojunction MODFET structure using atomic doping technique [6]. The high breakdown voltage, low light sensitivity, high transconductance and better control of threshold voltage make planar-doped MODFET structures very attractive for

large-signal applications such as high-efficiency millimeter-wave power amplification and high speed digital circuits.

To provide the basis for the development of integrated circuits using planar-doped MODFETs, a good large signal model is needed. The standard silicon JFET model or phenomenological equation using fitting parameters [7] available in existing circuit simulators such as SPICE may provide a good fit to GaAs MESFETs. However, the characteristic transconductance (g_m) compression of MODFETs at high gate bias is impossible to be simulated with a MESFET model whose g_m does not decrease with V_{gs}. This makes the analysis of certain important circuit performance, such as harmonic distortions in microwave power amplifiers and noise margins of digital circuits, practically impossible. A few good DC charge control models had been developed for both normal MODFET structures [8] [9] and inverted structures [10] with a uniformly doped AlGaAs layer. In this chapter, simple charge control models will be derived for normal single heterojunction MODFET structures and double heterojunction structures with planar-doped AlGaAs layers. These charge control equations will be very useful to be implemented in a circuit simulator to obtain the full current-voltage characteristics of the MODFET with a two-region model [9], with fully analytical equations [11], or with a phenomenological model [12]. The model developed here is based on AlGaAs/GaAs material system. It can also be used to describe the charge control of other planar-doped modulation-

doped structures such as pseudomorphic AlGaAs/InGaAs/GaAs systems or AlInAs/GaInAs/InP systems without losing generality.

2.2. Single Heterojunction MODFETs

Using the effective mass approximation and solving the one-dimensional Schrodinger's equation for the infinite triangle well along z-axis perpendicular to the heterointerface, the electron wavefunction confined at i-th state are the standard Airy function as obtained by Stern and Howard [13].

$$\Phi_i = A_i \left(\frac{2m^* qF}{\hbar^2}\right)^{1/3} \left[z - \frac{E_i}{qF} \right] , \tag{2.1}$$

where i=1,2,3, $\cdots$, q is the electronic charge, F is the effective electric field in the quantum well, and

$$E_i = \left(\frac{\hbar^2}{2m^*}\right)^{1/3} \left[\frac{3}{2}\pi qF\left(i + \frac{3}{4}\right)\right]^{2/3} , \tag{2.2}$$

is the quantized energy for the i-th subband. Applying the Gauss's law, that is

$$\varepsilon_1 F = q n_s \tag{2.3}$$

and assuming electrons are only occupying the ground (E_0) state and the first excited state (E_1), then

$$E_0 = 2.5x10^{-12}\ n_s^{2/3}\ \ (eV \cdot m^{4/3}) , \tag{2.4}$$

$$E_1 = 3.2x10^{-12}\ n_s^{2/3}\ \ (eV \cdot m^{4/3}) , \tag{2.5}$$

and

$$n_s = \frac{qm^*}{\pi\hbar^2}\ ln\left[\left(1+e^{\frac{q(E_F-E_0)}{kT}}\right)\left(1+e^{\frac{q(E_F-E_1)}{kT}}\right)\right] , \tag{2.6}$$

where

ε_1 is the permittivity of GaAs,

n_s is the sheet charge carrier density in the 2DEG,

and E_F is the Fermi level at equilibrium with respect to the conduction band of the GaAs at the heterointerface.

Fig. 2.1 shows the conduction band diagram perpendicular to the heterointerface. Neglect the contribution from the background impurity and assume the Schottky gate is located at z=+∞ pinned at the mid-bandgap, the one-dimensional Poisson's equation in the AlGaAs layer perpendicular to the heterointerface is

$$\frac{d^2V}{dz^2} = \frac{q}{\varepsilon_2}[\, n(z) - N_d^+(z)] \,, \tag{2.7}$$

where n(z) is the free electron concentration which can be approximated as [14]

$$n(z) = \frac{N_C e^{\frac{qV}{kT}}}{1+\frac{1}{4}e^{\frac{qV}{kT}}} \,, \tag{2.8}$$

and $N_d^+(z)$ is the ionized donor density of the activated planar-doped AlGaAs layer with a sheet doping density N_d and donor activation energy E_d

$$N_d^+(z) = \frac{N_d\, \delta(z)}{1+ge^{\frac{E_d+qV}{kT}}}. \tag{2.9}$$

V(z) is electrostatic potential relative to the Fermi level E_F, k is the Boltzmann constant, ε_2 is the permittivity of AlGaAs layer, g is the degeneracy factor of the donor level, T is the lattice temperature, and $\delta(z)$ is the Dirac delta function.

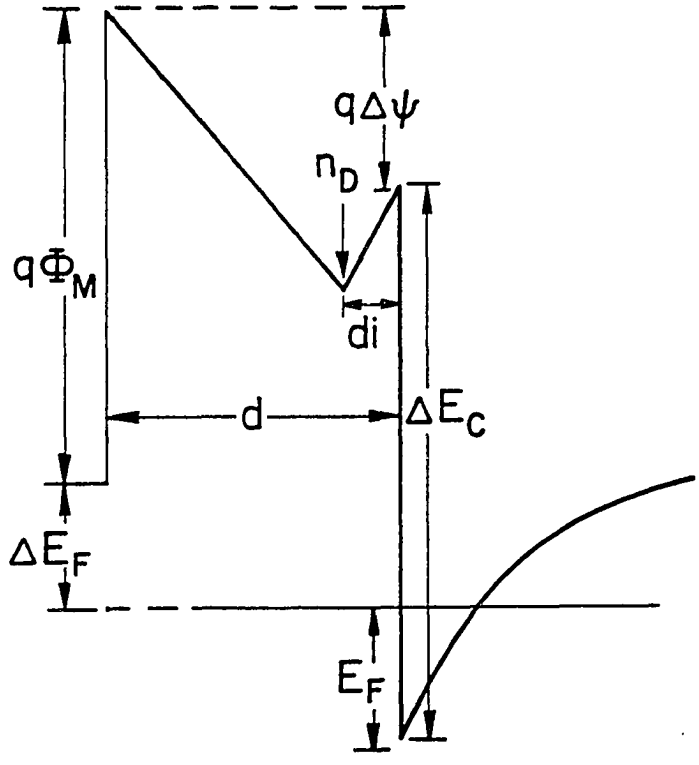

Figure 2.1. Conduction band diagram with a Schottky gate.

Integrating both side of Eq. 2.7 from z=+∞ to $z=d_i^+$ with respect to V with the boundary condition $V(+\infty)=E_g/2q$, $V(d_i)=\delta/q$, and $F(+\infty)=0$ at the gate, we have the electrical field at $z=d_i^-$

$$F(d_i^+) = \left[\frac{8N_C kT}{\varepsilon_2} \ln \frac{4+e^{\delta/kT}}{4+e^{E_g/2kT}}\right]^{1/2}, \tag{2.10}$$

at thermal equilibrium. Applying the Gauss's law at $z=d_i$, the electrical field at $x=d_i^-$ is

$$F(d_i^-)=F(d_i^+)-\frac{qN_d}{\varepsilon_2(1+ge^{\frac{E_d+\delta}{kT}})} . \tag{2.11}$$

Integrate both sides of Eq. 2.7 again over the region from $z=d_i^-$ to z=0, the electrical field at the AlGaAs side of heterojunction can be obtained

$$F(0^+) = -\left[F^2(d_i^-) + \frac{8N_C kT}{\varepsilon_2} \ln \frac{4+e^{\frac{\Delta E_c - E_F}{kT}}}{4+e^{\frac{\delta}{kT}}}\right]^{1/2} . \tag{2.12}$$

Using the Gauss's law at the heterojunction, the sheet density of 2DEG can be found as

$$n_{s0} = \left(\frac{\varepsilon_2}{q}\right)\left[F^2(d_i^-) + \frac{8N_C kT}{\varepsilon_2} \ln \frac{4+e^{\frac{\Delta E_c - E_F}{kT}}}{4+e^{\frac{\delta}{kT}}}\right]^{1/2} . \tag{2.13}$$

The equilibrium 2DEG density n_{s0} and the Fermi level E_F can be obtained by solving Eq. 2.6 and Eq. 2.13 simultaneously by an iterative computer program with

$$\delta = \Delta E_c - E_F - \frac{q^2 n_{s0} d_i}{\varepsilon_2} \quad . \tag{2.14}$$

The 2DEG density can be approximated as a linear function of the Fermi level

$$E_F = a\, n_s + E_{F0}, \tag{2.15}$$

where a and E_{F0} are fitting parameters such as in [15]. By solving the Poisson equation, ΔE_F can be expressed as

$$\Delta E_F = q\Phi_M + E_{F0} + a n_s + \frac{q^2 n_s d}{\varepsilon_2} - \Delta E_C - \frac{q^2 (d - d_i) N_d}{\varepsilon_2} \tag{2.16}$$

where n_s is the sheet density of 2DEG in the quantum well. The threshold voltage of this MODFET can be obtained by assuming $n_{s0}=0$ in Eq. 2.16, and is

$$V_{th} = \Phi_M + \frac{E_{F0}}{q} - \frac{\Delta E_C}{q} - \frac{q N_d (d - d_i)}{\varepsilon_2} \quad . \tag{2.17}$$

In contrast to the square law dependence between V_{th} and $(d-d_i)$ for conventional MODFETs with uniformly doped AlGaAs layer, the threshold voltage of planar-doped MODFETs varies linearly with $(d-d_i)$. This makes the planar-doped MODFETs very useful for large scale integration, where they offer tighter control of the uniformity of FET characteristics across the wafer and less sensitive to variations of the processing and growth parameters.

From the band diagram in Fig. 2.1, the difference between the quasi-Fermi level in the gate and in the two-dimensional channel is

$$\Delta E_F(x) = E_{FG} - E_F(x) = \Delta E_C - (q\Phi_M - q\Delta\Psi) \quad , \tag{2.18}$$

where x is any point in the intrinsic channel between the source and drain

underneath the gate, and

$$\Delta\Psi = \frac{qN_d(d-d_i)}{\varepsilon_2} - \frac{qn_s(x)d}{\varepsilon_2} \quad . \tag{2.19}$$

Eq. 2.15 can also be generalized to any position x under the gate as

$$E_F(x) = a \cdot n_s(x) + E_{F0} \quad . \tag{2.20}$$

A potential function $V(x)$ can be defined as

$$\Delta E_F(x) = -qV_G + qV(x) \tag{2.21}$$

along the channel, because

$$\Delta E_F(0) = -qV_G, \text{ and} \tag{2.22a}$$

$$\Delta E_F(L) = -qV_G + qV_D \tag{2.22b}$$

for intrinsic nodal voltages V_G and V_D without other FET parasitics such as R_s, R_d, etc.

If all of the donor atoms are ionized in the thin AlGaAs layer, the charge control equation of the 2DEG can be obtained by combining Eq. 2.16-2.21 into

$$n_s(x) = \frac{C_0}{q}(V_G - V_{th} - V(x)), \tag{2.23}$$

where

$$C_0 = \frac{\varepsilon_2}{d+\Delta d} \quad , \tag{2.24}$$

$$\Delta d = \frac{a\varepsilon_2}{q^2} \quad , \tag{2.25}$$

with a maximum 2DEG sheet density of

$$n_{s0} = \frac{\varepsilon_2(\Delta E_C - \delta - E_{F0})}{a\varepsilon_2 + q^2 d_i} \quad . \tag{2.26}$$

Eq. 2.23 describes the charge control equation in the two-dimensional channel of a planar-doped MODFET when the AlGaAs layer is fully depleted. There are no two-dimensional electrons accumulated in the channel when the gate bias is less than V_{th}. n_s increases with the gate bias till a critical gate voltage V_c is reached and electrons starts to build up in the AlGaAs layer. When the gate bias exceeds V_c, the 2DEG density remains at n_{s0} and the gate signal starts to modulate the low mobility AlGaAs MESFET channel [16]. The performance of the MODFET such as the transconductance (g_m) and the current gain cut-off frequency (f_T) will be degraded by this low-velocity low-mobility parallel conducting AlGaAs MESFET. The critical gate voltage V_c at the on-set of a parasitic AlGaAs channel can be obtained by inserting n_{s0} from Eq. 2.26 into Eq. 2.23, then

$$V_c = V_{th} + \left[\frac{d+\Delta d}{d_i+\Delta d}\right]\left[\frac{\Delta E_C - \delta - E_{F0}}{q}\right] \quad . \tag{2.27}$$

The charge control of the parasitic AlGaAs MESFET can be obtained by solving the one-dimensional Poisson equation between the Schottky gate and the heterointerface with a saturated 2DEG density of n_{s0}. The charge control equation of the planar-doped AlGaAs MESFET is governed by

$$n_s^*(x) = \frac{C^*}{q}(V_G - V_{th}^* - V(x)) \quad , \tag{2.28}$$

where $n_s^*(x)$ is the sheet electron density at a position x along the AlGaAs

MESFET channel with

$$C^* = \frac{\varepsilon_2}{d-d_i} \quad , \tag{2.29}$$

and

$$V_{th}^* = \Phi_M - \frac{\Delta E_C}{q} + \frac{an_{s0}}{q} + \frac{E_{F0}}{q} + \frac{qdn_{s0}}{\varepsilon_2} - \frac{qN_d(d-d_i)}{\varepsilon_2} \quad . \tag{2.30}$$

Once the charge control of the planar-doped MODFET structure is established for both the 2DEG channel (Eq. 2.23 at $V_G<V_c$) and the parasitic AlGaAs channel (Eq. 2.26 and 2.27 at $V_G>V_c$), the whole FET current-voltage characteristics can be calculated with one of the methods as demonstrated in [9], [11], or [12].

2.3. Double Heterojunction MODFETs

Although single heterojunction MODFETs have shown excellent microwave performance especially for low-noise amplifications [17], their current driving capability is limited to the available 2DEG sheet density less than $10^{12}cm^{-2}$. Many experimental investigations have been performed to improve the total 2DEG density by utilizing double or multiple heterojunction structures. Current density of 720 mA/mm from a double heterojunction structure [18] and 1100 mA/mm from a double quantum-well structure [19] have been reported. Combining the high current density of the multiple heterojunction structure and the high breakdown voltage with planar-doping techniques, these structures are very promising to fulfill the needs for millimeter-wave power amplifications and high-speed digital integrated circuits. In this section, the charge control mechanism in

planar-doped double heterojunction MODFETs will be studied. This also provides a basis to understand the operation principles of multiple heterojunction MODFET structures.

The conduction band diagram of a DH-MODFET structure is shown in Fig. 2.2. From the band diagram, the difference between the quasi-Fermi level of the gate and the channel is

$$\Delta E_F = q\Delta\Psi - q\Phi_M + (\Delta E_{C2} - \Delta E_{F2}) \quad , \tag{2.31}$$

where

$$\Delta E_F = -qV_G + qV(x) \tag{2.32}$$

and V(x) is the potential at position x in the FET channel. By solving the Poisson equation perpendicular to the heterointerface (z-axis),

$$\Delta\Psi = \frac{qd(-n_s + N_{d1})}{\varepsilon_2} + \frac{qN_{d2}(d - d_{l2})}{\varepsilon_2} \quad , \tag{2.33}$$

where n_s is the sheet density of 2DEG, N_{d1} and N_{d2} are the sheet doping densities in the bottom and top AlGaAs layer respectively, d_1 and d_2 are the thickness of bottom and top undoped spacer layers. Combining Eq. 2.31-2.33 and assuming

$$\Delta E_{C2} = \Delta E_{C1} + \beta \quad , \tag{2.34}$$

the charge control equation along the 2DEG channel (x-axis) is

$$n_s(x) = \tag{2.35}$$

$$\frac{\varepsilon_2}{qd}\left[V_G - V(x) - \Phi_M + \frac{\beta + \delta}{q} + \frac{qN_{d1}(d_{l1} + d)}{\varepsilon_2} + \frac{qN_{d2}(d - d_{l2})}{\varepsilon_2} + \frac{\Delta E_{F1}(x) - \Delta E_{F2}(x)}{q}\right] .$$

ΔE_{F1} and ΔE_{F2} are separations between the Fermi level and the conduction

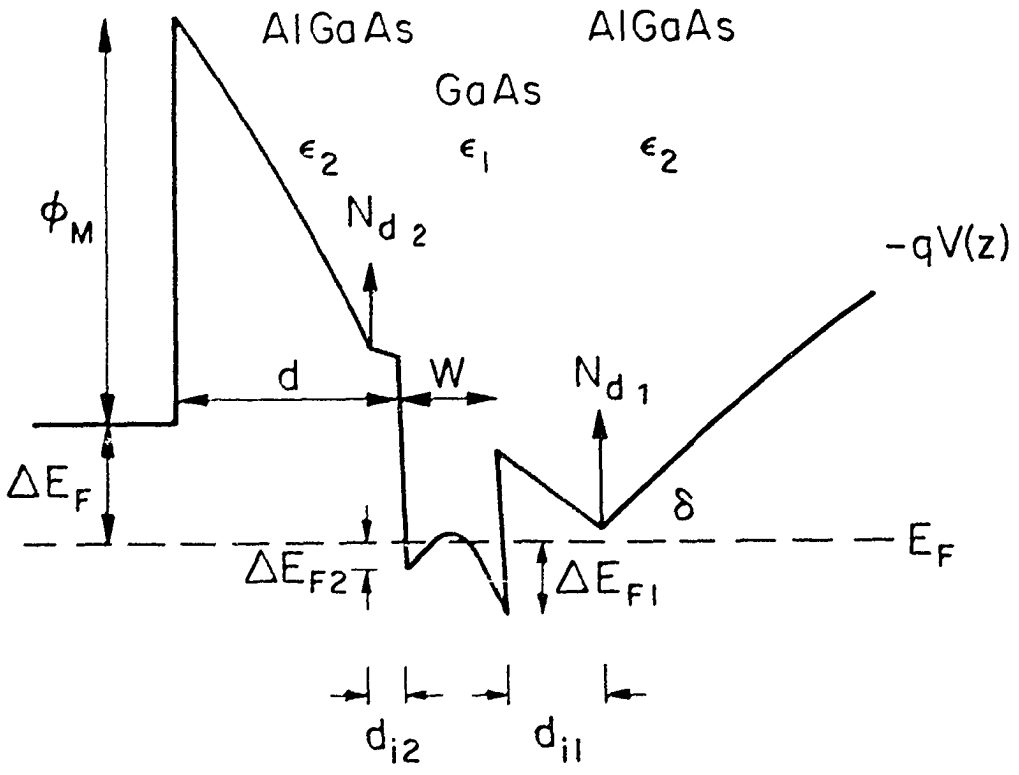

Figure 2.2. Conduction band diagram of a DH-MODFET structure.

band minimums at the bottom and top heterointerface, where

$$\Delta E_{F1} = \Delta E_{C1} - \delta - \frac{q^2 N_{d1} d_{l1}}{\varepsilon_2} \quad . \tag{2.36}$$

Eq. 2.35 and 2.36 is usually solved by an iterative quantum mechanical self-consistent calculation such as in [20]. If we only consider the charge control of the double heterojunction diode structure, $V(x)=0$ can be inserting into Eq. 2.35 which corresponds to the source end of the channel. Then the charge control equation is simplified to

$$n_s = \frac{\varepsilon_2}{qd}\left[V_G - \Phi_M + \frac{\beta+\delta}{q} + \frac{qN_{d1}(d_{l1}+d)}{\varepsilon_2} + \frac{qN_{d2}(d-d_{l2})}{\varepsilon_2} + \frac{\Delta E_{F1}-\Delta E_{F2}}{q}\right] \tag{2.37}$$

For any given V_G, the sheet density of 2DEG (n_s) can be solved with a iterative program by combining Eq. 2.35, 2.36, and 2.37 under the assumption that all the AlGaAs layers are depleted.

The threshold voltage of the DH-MODFET can be determined by Eq. 2.37 with $n_s=0$ and $\Delta E_{F1}-\Delta E_{F2}=q^2 N_{d1} W/\varepsilon_1$, and is

$$V_{th\ DH} = \Phi_M - \left[\frac{\beta+\delta}{q} + \frac{qN_{d1}(d_{l1}+d)}{\varepsilon_2} + \frac{qN_{d2}(d-d_{l2})}{\varepsilon_2} + \frac{qN_{d1}W}{\varepsilon_1}\right] , \tag{2.38}$$

if the electrical field in the substrate is negligible and W is the width of the quantum well. Again, the threshold voltage of the planar-doped double hetero-junction MODFETs is a linear function of the thickness of each layer. They inherit all the advantages of the planar-doped single heterojunction MODFET such as high breakdown voltage, high transconductance, processing stability,

and enhanced power efficiency, plus higher current density and better electron confinement under high drain field.

2.3.1. Wide Quantum-Well

Although an iterative computer program (such as the one used in Chap. 4) is needed to solve the charge control problems in a DH-MODFET, it is interesting to examine a few special charge control problems analytically. For a DH-MODFET structure with a wide quantum well, two heterointerface notches may be treated separately. Under this assumption, the charge control problem may be treated analytically instead of going through an iterative self-consistent program as in [20].

(1) $V_{th\,DH} < V_G < V_{p1}$

If $V_G < V_{th\,DH}$, all the free carriers are depleted by the reverse-biased Schottky gate, and there is no current flowing in the channel. As the gate bias is raised above the threshold voltage $V_{th\,DH}$, electrons start to fill in the bottom heterointerface. Assuming the top heterointerface is fully depleted in the wide quantum-well and all the donor atoms in AlGaAs layers are ionized, the charge control at the bottom interface can be obtained from Eq. 2.37 together with the boundary condition

$$\Delta E_{F1} - \Delta E_{F2} = \frac{q^2 W}{\varepsilon_1}(N_{d1} - n_s) \quad . \tag{2.39}$$

The charge control equation is then

$$n_s = \frac{C_1}{q}(V_G - V_{th\,DH}) \quad , \tag{2.40}$$

with

$$C_1 = \frac{1}{\frac{d}{\varepsilon_2} + \frac{W}{\varepsilon_1}} \quad , \tag{2.41}$$

where W is the width of the quantum-well channel.

If the doping density and the layer thickness of the top planar-doped AlGaAs layer are set to zero, Eq. 2.41 is the charge control equation for an inverted MODFET [10]. The maximum amount of electrons can be transferred from the bottom AlGaAs layer is limited to the ionized silicon donor density N_{d1}. If the width of the quantum well is very wide or N_{d1} is low, the bottom triangle notch will be filled up first before electrons start filling in the top notch. Under this situation, $n_{s1}=N_{d1}$, the critical voltage V_{p1} is

$$V_{p1} = \frac{qN_{d1}}{C_1} + V_{th\,DH} \quad . \tag{2.42}$$

(2) $V_{p1}<V_G<V_{G0}$

If the 2DEG density in bottom notch is saturated at N_{d1} before the electrons start to fill in the top interface, then a linear relation between ΔE_{F2} and n_{s2} can be assumed for the top interface notch as in [9]:

$$\Delta E_{F2} = a^* N_{s2} + b^* \quad , \tag{2.43}$$

with $n_{s2}=N_{d1}$, where a^* and b^* are fitting parameters. This assumption can be justified at low gate bias by examining the simulated E_F–n_s data for a DH-

MODFET structure with a 300 A quantum well based on the self-consistent calculation [20] where a^* is in the order of $0.125x10^{16}$ eV-cm^2. Then, for the DH-MODFET structure structure shown in Fig. 2.2, the charge control equation for a very wide quantum-well width (W) can be derived as by combining Eq. 2.37, 2.38, and 2.43 into

$$n_s = n_{s1}+n_{s2} \tag{2.44}$$

$$=N_{d1} + \frac{C_2}{q}(V_G - V_{p2}) \ ,$$

where

$$C_2 = \frac{1}{(\frac{d}{\varepsilon_2}+\frac{a^*}{q^2})} \ , \tag{2.45}$$

and

$$V_{p2} = V_{th\ DH} - \frac{\Delta E_{C1} - \delta - b^*}{q} + \frac{qN_{d1}(d+d_{i1})}{\varepsilon_2} + \frac{qN_{d1}W}{\varepsilon_1} \ . \tag{2.46}$$

The sequential filling first the bottom heterointerface and then the top heterointerface will result in two distinctive plateaus in the capacitance-voltage characteristics of the DH-MODFET structure as depicted in Fig. 2.3. The capacitance of a Schottky diode will increase from nil to the first plateau of C_1 when the gate bias is higher than $V_{th\ DH}$. Between $V_{th\ DH}$ and V_{p1}, the bottom heterointerface is charging up with a capacitance of C_1. Once the area of the first plateau (i.e. area=$C_1(V_{p1}-V_{th\ DH})$,) equals qN_{d1}, the electrons start filling in the top heterointerface. This results in a second plateau of a value C_2 until the

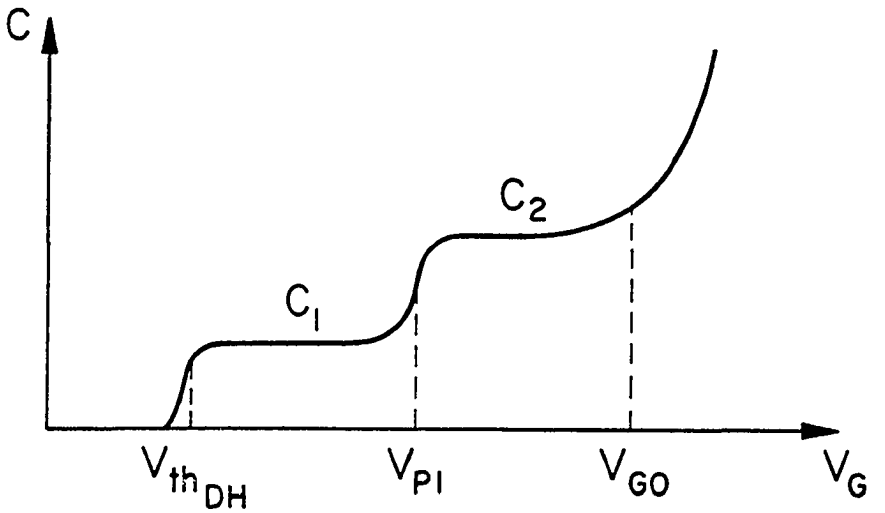

Figure 2.3. Ideal capacitance-voltage curve of a DH-MODFET with a wide quantum well.

parasitic charges begin to build up in the top AlGaAs layer at $V_G \cong V_{G0}$. The maximum sheet density of 2DEG will be the area underneath the C-V curve from $V_{th\ DH}$ to V_{G0}. The charge control of the planar-doped DH-MODFET at the plateaus will be governed by Eq. 2.40 and 2.44. Although it is interesting to observe the charge control of this kind of DH-MODFET structures with distinctive regions, this will result in non-linear g_m–V_G relations, where

$$g_m = \frac{\partial i_D}{\partial V_G} \quad . \tag{2.47}$$

It is very undesirable to have a non-linear $g_m(V_G)$ characteristics for the large-signal power amplifications, because higher order harmonics will be generated and the efficiency of the device will be degraded.

2.3.2. Narrow Quantum-Well

In designing practical multiple heterojunction power MODFETs, thin quantum wells are used to improve the linearity of the G_m characteristics as well as to improve the gate-to-buffer aspect ratio for high frequency gains, particularly for FETs with submicron gate-length. When the DH-MODFET with thin quantum-well is operated near the pinch-off, the charge control equation (Eq. 2.40) may still be applicable. However, the criterions and assumptions we used for a structures with wide quantum wells will no longer be correct when both notches start accumulating electrons. In this case, more rigorous equations such as Eq. 2.37 should be used.

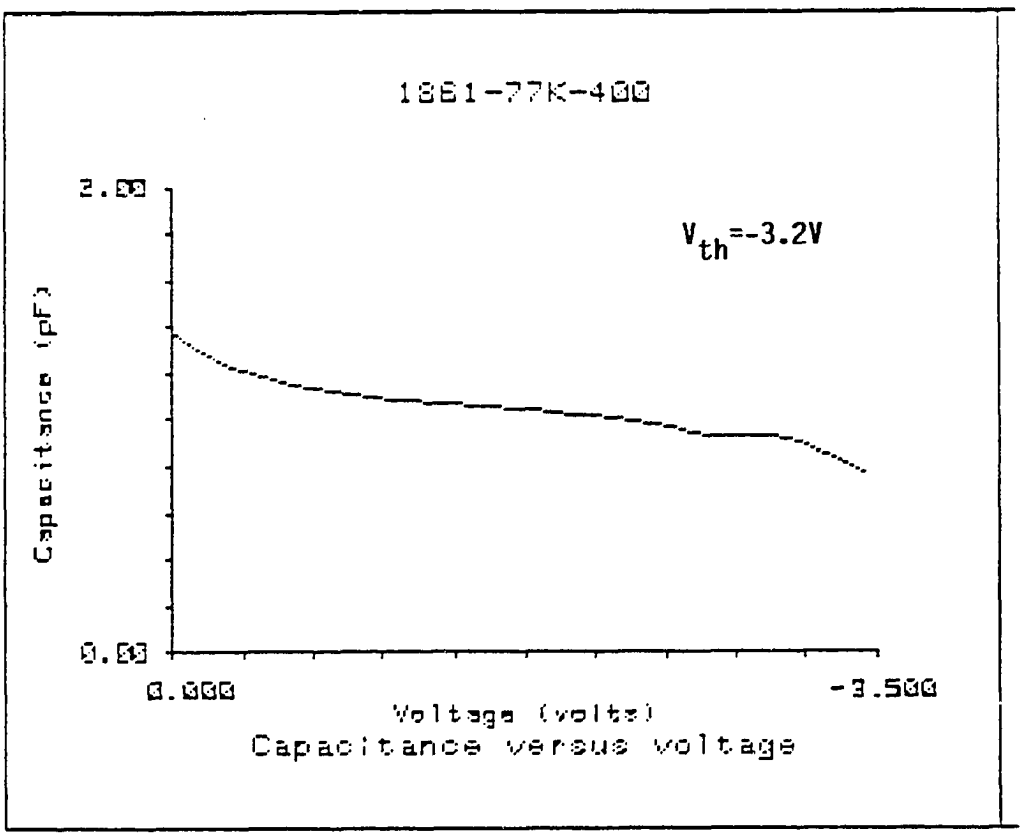

Figure 2.4. Measured 77K capacitance-voltage curve of a DH-MODFET with 250 A quantum-Well.

Under this situation, the transition between the two plateaus in the C-V characteristics will not be obvious, and it is usually smeared out as a monotonic increasing function of gate voltage. Fig. 2.4 shows a measured C-V curve at 77 K from a DH-MODFET structure with 250 A quantum well. Nevertheless, part of the first plateau is still visible near the pinch-off.

2.4. Figures-of-Merit

Because the real FET operation involves both the charge control mechanism and various transport dynamics, a two-dimensional numerical model is also needed to determine the electron potential $V(x)$ along the channel under various gate and drain biases. The static charge control model is not sufficient to predict the dynamic FET characteristics. However, a simple linearized two-piece mobility-field relationship for 2DEG as in [9] is assumed to estimate some figures-of-merit based on the derived charge control model.

2.4.1. Small-Signal Transconductance

The channel current and transconductance at on-set of drain current saturation (i.e. $V(L)=V_c=LF_c$) can be obtained as

$$I_D = \frac{qZ}{L}\int_0^L n(x)v(x)\,dx \qquad (2.48)$$

$$= \frac{C_p \mu Z V_c^2}{L}\left[\sqrt{1+\left(\frac{V_G-V_{th}}{V_c}\right)^2}-1\right]$$

and

$$g_m = \frac{\partial I_D}{\partial V_G} \qquad (2.49)$$

$$= \frac{C_p \mu Z}{L}(V_G - V_{th}) \left[1+(\frac{V_G - V_{th}}{V_c})^2\right]^{-1/2} ,$$

where a capacitive charge control model

$$n_s(x) = \frac{C_p}{q}(V_G - V(x) - V_{th}) \qquad (2.50)$$

is used, μ is the low-field mobility, F_c is the critical field for the onset of saturated velocity v_s, Z and L are the gate width and the effective gate length at $V(L)=V_D$ of the MODFET. It can be seen from Eq. 2.49, that the transconductance increases with the gate bias before electrons start to accumulate in the AlGaAs layer. At low V_G, g_m increases as the gate-length is reduced. However, it will reach a maximum at high V_G for a very short gate-length ($L \approx 0$) with a value of

$$g_{m,max} = Z v_s C_p \ , \qquad (2.51)$$

where an average saturation velocity v_s is assumed.

(1) Single Heterojunction MODFET

The transconductance of single heterojunction MODFET can be described by Eq. 2.49 as long as the top AlGaAs layer is totally depleted. The maximum value of g_m can possibly be obtained can be calculated from Eqs. 2.23 and 2.51, and is

$$g_{m,max} = \frac{qZv_s}{(\frac{d}{\varepsilon_2}+\frac{a}{q^2})} \quad . \tag{2.52}$$

High transconductance can be achieved by shrinking the gate length as well as the thickness of the planar-doped AlGaAs layer. This can not be done in the conventional MODFET structures with uniformly-doped AlGaAs electron supplying layer without degrading the full channel current or breakdown voltage. The threshold voltage can also be reduced with the thinner AlGaAs layer. High transconductance together with low FET threshold voltage enhances the linear gain at all frequencies and requires less input power to drive the MODFET in the large signal amplifications. Combine these with the improved gate-to-drain breakdown voltage in the planar-doped AlGaAs layer of low surface doping density, the planar-doped MODFET is a very promising candidate for millimeter-wave power amplifications with high gain and high efficiency.

(2) Double Heterojunction MODFET

The dynamic charge control in DH-MODFETs under a drain bias is very complicated. Even though we may simplify the wide quantum-well structure as a pair of decoupled triangle wells to study the static charge control problem, the quasi-Fermi level will change along the heterointerface between the source and the drain and they can no longer be treated separately under a drain potential. An iterative numerical program is needed to solve this one-dimensional problem. In the absence of a decent numerical program, experimental techniques,

such as DC, RF, and optical measurements, are used to study the behaviors of DH-MODFET structures, although a good computer program includes all possible mechanisms is invaluable [21].

From the experimental g_m data from a DH-MODFET structure with 250A quantum well, two transconductance peaks may be observed as shown in Fig. 2.5. The first peak is the result of charge accumulation in the bottom inverted interface, and its zero gate-length maximum value can be calculated from Eq. 2.41 and 2.51

$$g_{ml,max} = \frac{qv_{sl}Z}{(\frac{d}{\varepsilon_2} + \frac{W}{\varepsilon_1})} \quad , \tag{2.53}$$

at a maximum drain current level of

$$I_{Dl,max} = qN_{d1}v_{sl} \quad . \tag{2.54}$$

The lower g_m between two peaks is the result of saturation of electron accumulation at the bottom heterointerface with an empty top heterointerface and the on-set of parasitic electrons in the bottom AlGaAs layer before the electrons start filling in the top heterointerface. The maximum g_m can be provided by the de-coupled top heterointerface can be estimated by solving Eq. 2.45 and 2.51,

$$g_{mN,max} = \frac{qv_{sN}Z}{(\frac{d}{\varepsilon_2} + \frac{a^*}{q^2})} \quad . \tag{2.55}$$

v_{sl} and v_{sN} are saturated electron drift velocities at the inverted and the normal interface in a wide quantum well. Usually, $v_{sl} < v_{sN}$ because of the difficulty of

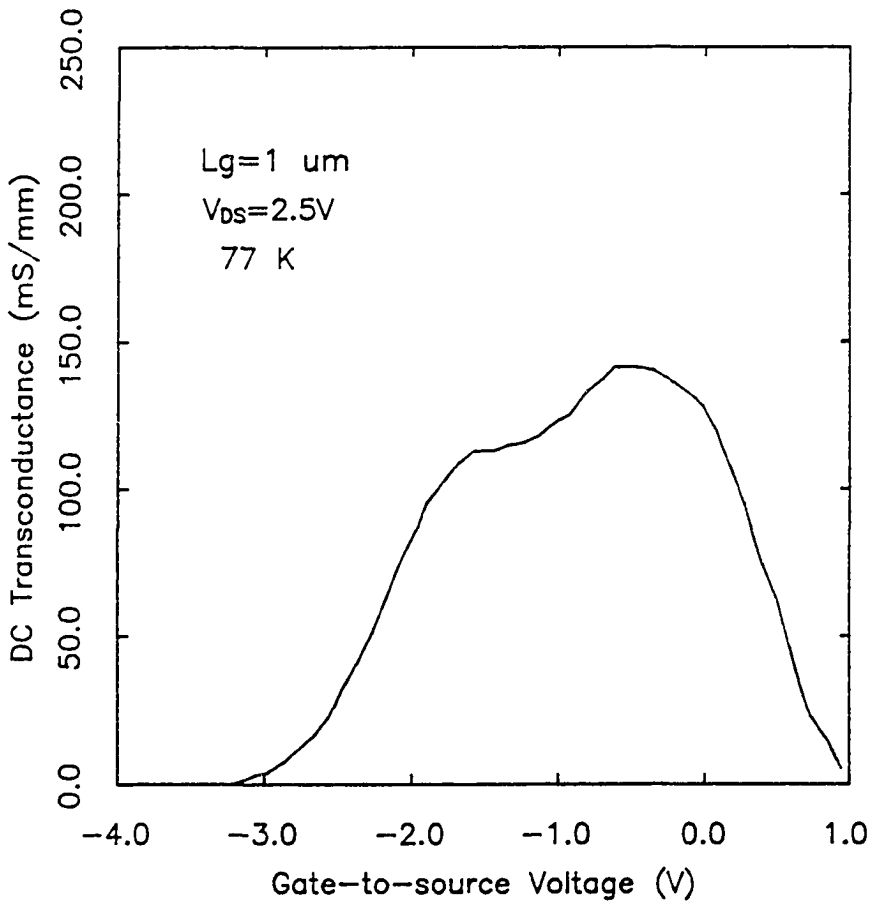

Figure 2.5. Measured 77K g_m vs V_g curve of a DH-MODFET with 250 A quantum well.

obtaining high quality bottom inverted heterointerface during the MBE growth. As the result of the lower drift velocity and farther separation between the gate and the inverted interface, g_{mI} is usually smaller than g_{mN}. It can be seen from Eq. 2.53 and 2.55 for a wide quantum well, the maximum transconductance may not be much higher than that of a single heterojunction MODFET despite the increase in the maximum channel current and power density. Thin quantum well thickness is needed to improve the transconductance, where both interfaces could contribute to the channel current under the gate modulation.

2.4.2. Current Gain Cut-Off Frequency

Current gain cut-off frequency f_T is a very important figure-of-merit which connects the high frequency performance of MODFETs with the quality of the grown material and the structure of heterojunction layers. Despite the distorted measured h_{21} data which could strongly affected by the device and circuit parasitics, the intrinsic f_T can be defined as

$$f_T = \frac{g_m}{2\pi C_{GS}} = \frac{\dfrac{\partial I_D}{\partial V_G}}{2\pi\left[\dfrac{\partial Q_{GS}}{\partial V_G}\right]} = \frac{\dfrac{\partial}{\partial V_G}\int_0^L n(x)\, v(x)\, dx}{2\pi L \dfrac{\partial}{\partial V_G}\int_0^L n(x)\, dx}\ , \qquad (2.56)$$

where x is the position in the intrinsic channel along the heterointerface, and L is the effective gate length under the external bias of V_G and V_D. If all the electrons are traveling with an averaged saturated velocity v_s (e.g. for a device with long gatelength), then

$$f_T = \frac{v_s}{2\pi L}. \tag{2.57}$$

In this formulation, v_s is a macroscopic parameter in much the same way as f_T and g_m, which is influenced by microscopic scattering mechanisms, the specific layered structure [21], and bias combinations being used. It is, however, possible to use Eq. 2.57 as a handy tool to study the transport and charge control properties of MODFET structures on the first principle basis.

For the lineraized two-piece *v–F* model used to derive Eqs. 2.48-2.50 under the depletion approximation, C_{gs} and f_T are

$$C_{gs} = \frac{C_p L(V_G - V_{th})}{V_c} \frac{(2-\frac{1}{\gamma})}{\left[(1+\gamma^2)^{1/2} - 1\right]}, \tag{2.58}$$

$$f_T = \frac{v_s}{2\pi L} \frac{\left[1-\frac{1}{\sqrt{1+\gamma^2}}\right]}{2-\frac{1}{\gamma}}, \tag{2.59}$$

where

$$\gamma = \frac{V_G - V_{th}}{V_c}. \tag{2.60}$$

From Eq. 2.59 for a short channel device at $V_D = V_c$,

$$f_T \approx \frac{v_s/2}{2\pi L}. \tag{2.61}$$

2.5. Summary

In this chapter, charge control models are derived for planar-doped MODFET structures with both single and double heterojunctions. Because of the

linear charge control in terms of the gate-to-channel spacing in the model, the threshold voltage and transconductance are less sensitive to the precessing and growth variations which are very important for large scale integration. The electrical field underneath the gate is determined by the location of the doping spike in top AlGaAs layer rather than the doping concentration itself as in the case of uniformly doped AlGaAs layer. The improved breakdown voltage is very important to enhance both the power density and efficiency of millimeter-wave power transistors.

Equipped with these basic charge control models, the dynamics of planar-doped MODFETs can be examined, which combines both charge control problems and carrier transport mechanisms. Because of the vast amount of assumptions and simplifications used in deriving these charge control models together with the complication from some unexposed transpsrt mechanisms, the following chapters utilize experimental approaches, such as DC, microwave, and optical measurement techniques, to study and improve layered structures of planar-doped MODFETs. More attentions will be directed to double-heterojunction MODFET structures because of their inherent large current densities. The study on DH-MODFETs will also be useful to understand the multiple heterojunction MODFETs.

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CHAPTER 3

BIAS-DEPENDENT MICROWAVE CHARACTERISTICS

3.1. Introduction

In order to perform computer simulation of high performance MODFET circuits, an accurate large signal model is needed. Although a few models had been successfully implemented to describe the DC current-voltage characteristics of MODFETs [1-3], very little study was done to investigate the variations of AC large signal behaviors of these devices. Because of the existence of slow trapping states in the substrate and the epitaxial layers [4], it is inaccurate to predict the high frequency characteristics of MODFETs based on the DC and low-frequency small-signal parameters. One commonly observed discrepancy is the frequency dependent output conductance at low frequencies. To examine the high frequency limit of MODFETs, the equivalent circuit model should be established with broad-band microwave characterization technique beyond 0.5 GHz.

In this chapter, a non-linear equivalent circuit model is investigated. The model parameters are experimentally determined by microwave scattering parameters from 0.5 GHz to 26.5 GHz at each bias point. Then the value of each non-linear parameter will be studied for their bias-dependence. These

results are of great importance in examining the MODFET device dynamics and in predicting the non-linear MODFET circuit performance such as the transient response, the power saturation characteristics, harmonic and intermodulation distortions. By closely examining the bias-dependent non-linear behavior, effects from distinctive MODFET characteristics (such as heterojunction charge control, AlGaAs parallel conduction, and real-space transfer) on its high frequency performance can be correlated, and the layer structure can then be optimized.

3.2. Layer Structure

Single heterojunction Modulation-Doped Field-effect Transistors (MODFETs) have demonstrated excellent microwave performance with very high cut-off frequency and very good low-noise performance [5]. However, their current driving capability are limited by their sheet charge density of less than $1.0x10^{12}cm^{-2}$, therefore their power performance and switching speed, which are directly related to current driving capability, were not much better than the MESFETs. Multiple heterojunction devices [6-10] were then investigated to increase the current density.

In this chapter, double heterojunction MODFET structures which utilize lattice-strained AlGaAs/InGaAs/GaAs modulation-doped structures will be characterized for their large signal behaviors. The planar-doping technique is utilized to place the silicon donors in both the top AlGaAs and the bottom GaAs

electron supplying layer. This doping profile offers good charge control of the 2DEG density as well as good break-down behavior with very little light sensitivity at low temperature (77 K) because of the much reduced region of the heavily doped AlGaAs layer [10].

The structure is grown by MBE on top of an semi-insulating GaAs substrate in the following sequence: 5000 A of superlattice buffer layer, 50 A undoped AlGaAs, Si doping plane with a density of $2x10^{12}cm^{-2}$, 85 A undoped AlGaAs, 200 A undoped InGaAs channel, 30 A undoped AlGaAs spacer layer, Si doping plane with a density of $6x10^{12}cm^{-2}$, 250 A undoped AlGaAs, and 400 A GaAs cap layer doped to $1x10^{18}cm^{-3}$. The mole fractions of aluminum and indium are 30% and 15% respectively.

3.3. Device Fabrication Process

The grown wafers are fabricated with a standard recess-gate FET process. The following paragraphs outlines the fabrication sequences which will be followed in most of work performed in this thesis except those for optical detectors in Chapter 6. The lithography of the first two steps, mesa level and ohmic level are defined by a mid-UV optical contact aligner (Karl Suss MJB/3 UV300). The light intensity is fixed at 10 mW/cm^2. Optical lithography is also used to form the gate level pattern with 1-μm dimension. For the submicrometer gate-length, the electron beam lithography is used to define the gate level pattern.

3.3.1. Mesa Level

Indium is removed from the backside of wafer first with HCl and then by mechanical lapping. The wafer is degreased with acetone and methanol before the 10-minute 110 C dehydration bake in a convection oven. The positive AZ4110 resist is spun on the wafer for 30 seconds with a spinner at 5000 rpm. Then the wafer is put in an oven for 20 minutes at 80 C. The thick resist bead on the edge of the wafer is removed in the following sequence: expose the wafer with a special mask for one minute, develop the wafer in (1:4) AZ400K:DI solution for one minute, rinse the wafer in DI water, and blow dry with N_2. Now the coated wafer surface is flat enough for intimate contact printing.

The mesa patterns are then defined by exposing the wafer again under the mesa mask for 40 seconds and developing in the (1:4) AZ400K solution for 40 seconds. A post-bake in 100 C oven for 30 minutes is needed to improve the adhesion of the resist against the long wet-chemical etching. The active epilayer between the active devices is etched away with a solution of H_3PO_4:H_2O_2:DI (4:1:50). The etching rate is in the order of 1000 A/min. The resist pattern is removed with acetone and methanol after the etching.

3.3.2. Ohmic Level

After device isolation is done by mesa etch, source and drain ohmic contacts patterns are defined by optical lithography again. The process of defining the ohmic patterns is the same as what have been used for the mesa level

except an added chlorobenzene soak process to facilitate the lift-off process. After the exposure, the wafer is soaked in chlorobenzene for 3 minutes and blown dry immediately with N_2 gas. The resist patterns are developed after 75 seconds in the (1:4) AZ400K solution. The wafer is then processed with 10 second oxygen plasma to remove the residue resist, and 15 second NH_3OH:DI (1:15) to strip the oxide before the wafer is loaded into the evaporator. Ni/AuGe/Ag/Au (80A/800A/1000A/1000A) are subsequently evaporated and lifted off in acetone.

Rapid thermal annealer (AG Heatpulse 410) was used to alloy the metals at 450C for 10 seconds to form the ohmic contacts. The characteristics of ohmic contacts are evaluated with a transmission line pattern. A typical specific contact resistivity of 0.1 ohm-mm is routinely obtained.

3.3.3. Gate Level

The mid-UV contact aligner is used to define the 1-μm gate, while the electron beam lithography is used to write the 0.3-μm gate pattern. In order to minimize the parasitic resistance in the submicrometer gate lines, a triple-level PMMA-P(MMA,MAA)-PMMA electron beam resist is developed to form the T-shape gate [11]. This resist system utilizes the thin bottom PMMA layer as the imaging layer to define the footprint, the thick high-sensitivity middle P(MMA-MAA) layer to form the top T-shape gate, and the top PMMA layer to provide good lift-off profile. Fig. 3.1 shows the SEM photomicrograph of a triple-layer

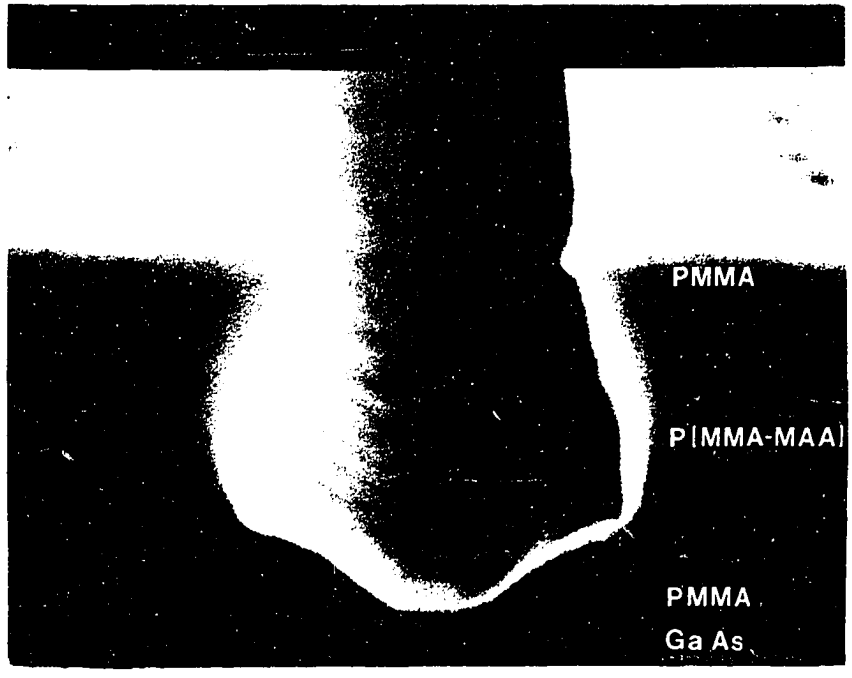

Figure 3.1. Cross-section view of a T-shaped opening of the triple layer PMMA-P(MMA,MAA)-PMMA resist system.

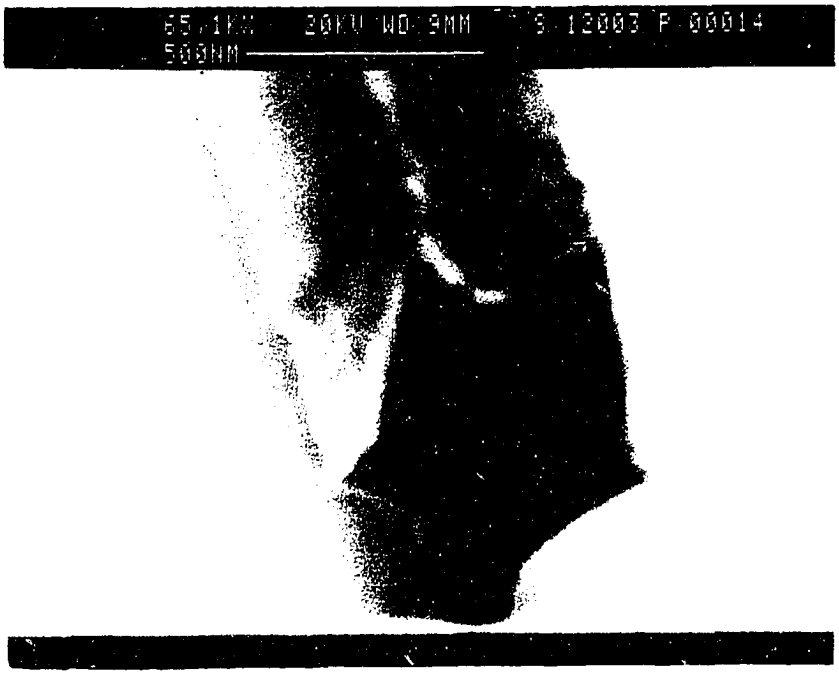

Figure 3.2. T-shaped gate line with a 0.12-μm footprint.

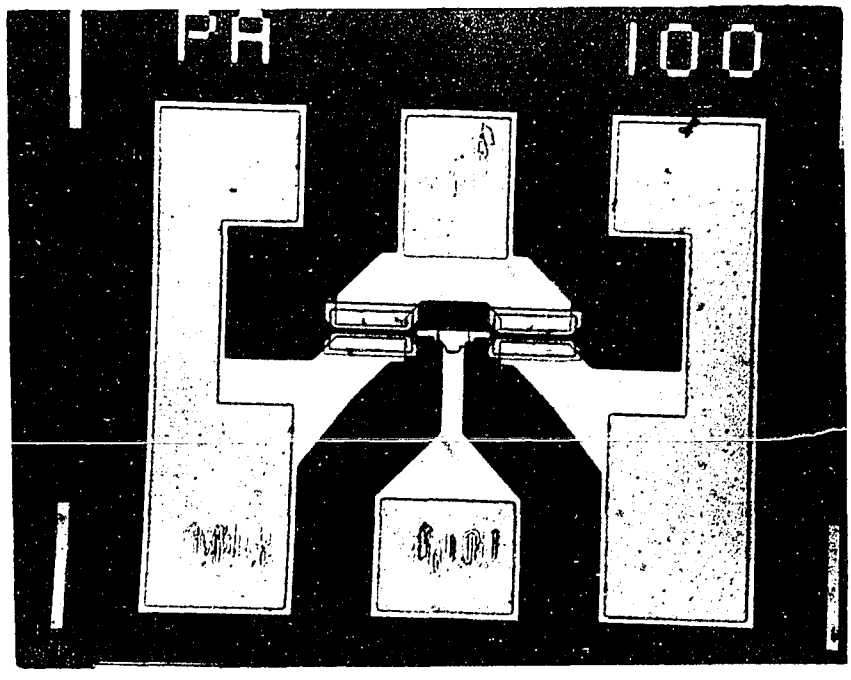

Figure 3.3. T-gate device layout for microwave probing.

resist profile after the exposure and development. A fine bottom resist opening of 0.1-μm can be seen. We utilize 0.3-μm footprint to characterize submicrometer-gate MODFETs, although MODFETs with 0.12-μm footprint can be demonstrated in Fig. 3.2 and in [12].

After the submicrometer gate patterns are defined, the GaAs cap layer is removed by recess etch and the channel current is also adjusted. After the oxygen descum and removal of surface oxide, Ti/Pd/Au (400A/400A/4500A) metal layers are deposited and lift-off. The gate resistance of the T-shape gate is in the order of 120 Ω/mm for 0.3-μm gate length which is obtained from both the DC end-to-end data and RF measurement. Fig. 3.3 shows a photomicrograph of a fabricated MODFET with 100-μm gate width. This layout is specifically tailored for the direct microwave probing on the wafer level.

3.4. DC Characteristics

Fig. 3.4 shows the room temperature I-V characteristics of a fabricated 1 X 100 μm MODFET. The peak extrinsic DC g_m is 400 mS/mm with a maximum channel current of 610 mA/mm. The I-V characteristics of a 0.3 X 100 μm MODFET is shown in Fig. 3.5. A peak extrinsic g_m of 505 mS/mm is obtained. This 0.3-μm device shows very good output conductance and pinch-off characteristics because of the improved carrier confinement in the quantum well [10].

Fig. 3.6 shows the conduction band diagram of the planar-doped quantum well structure. The threshold voltage (V_T) of the double heterojunction

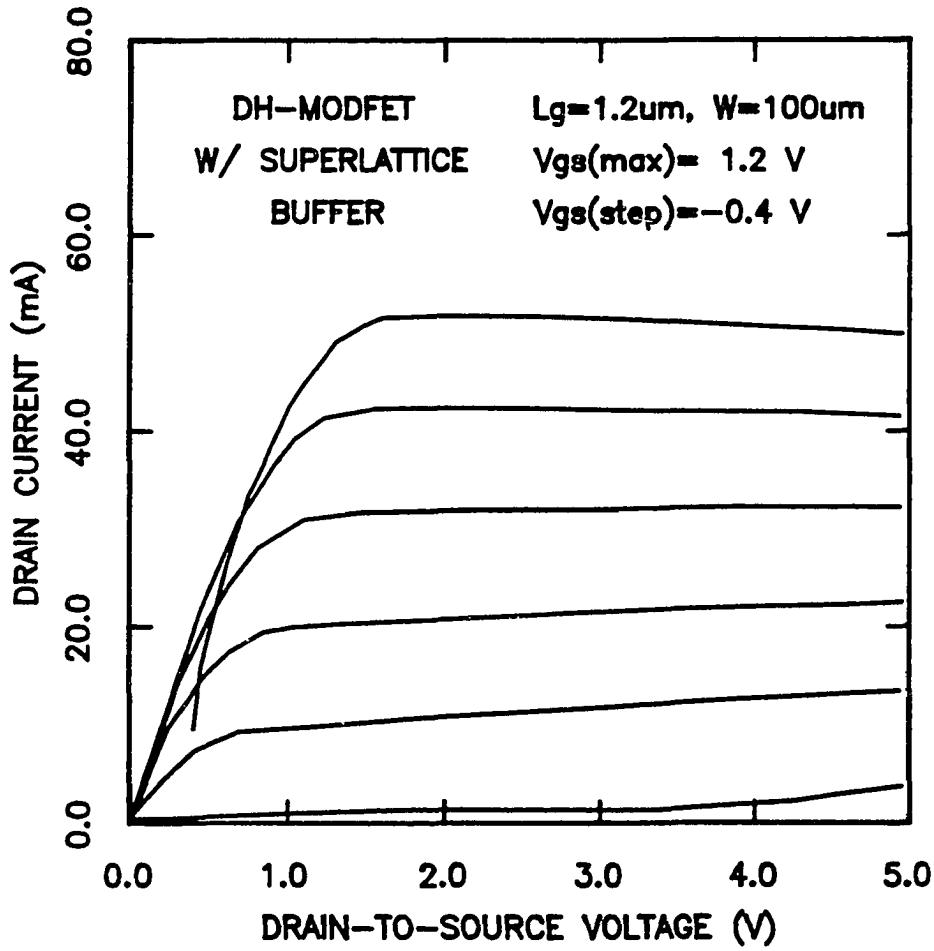

Figure 3.4. I-V characteristics of a 1X100 μm MODFET.

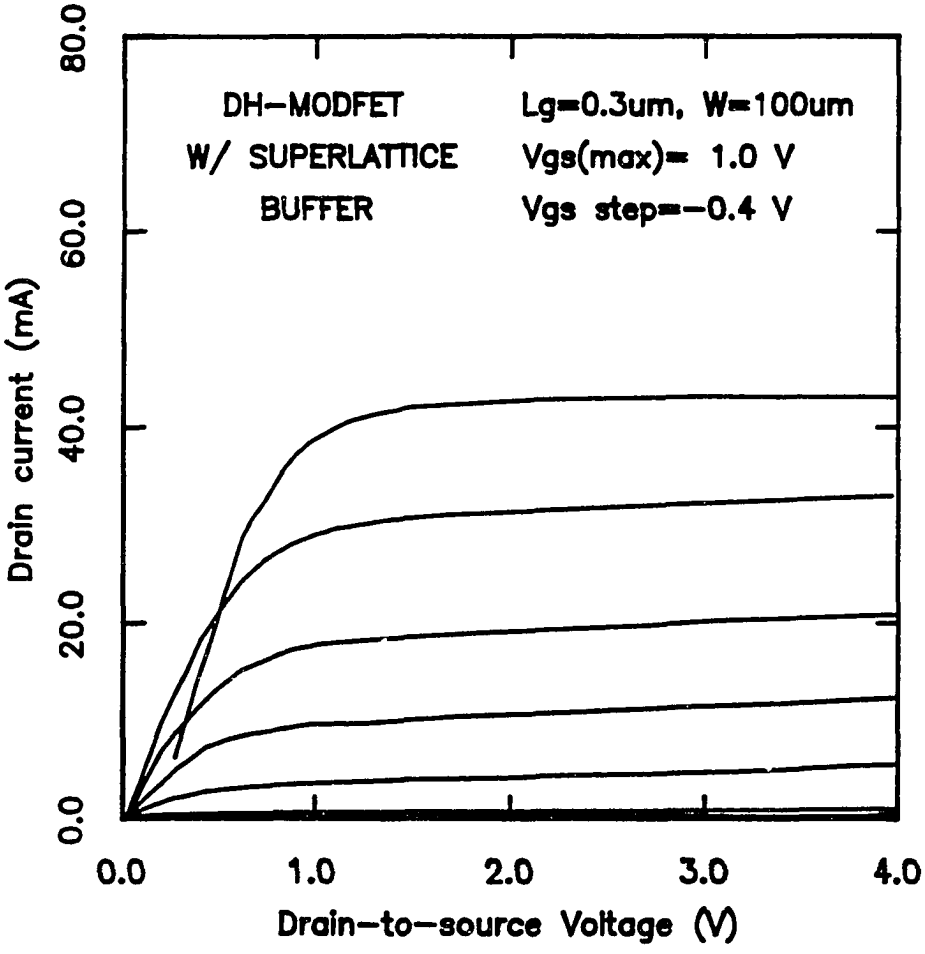

Figure 3.5. I-V characteristics of a 0.3x100 μm MODFET.

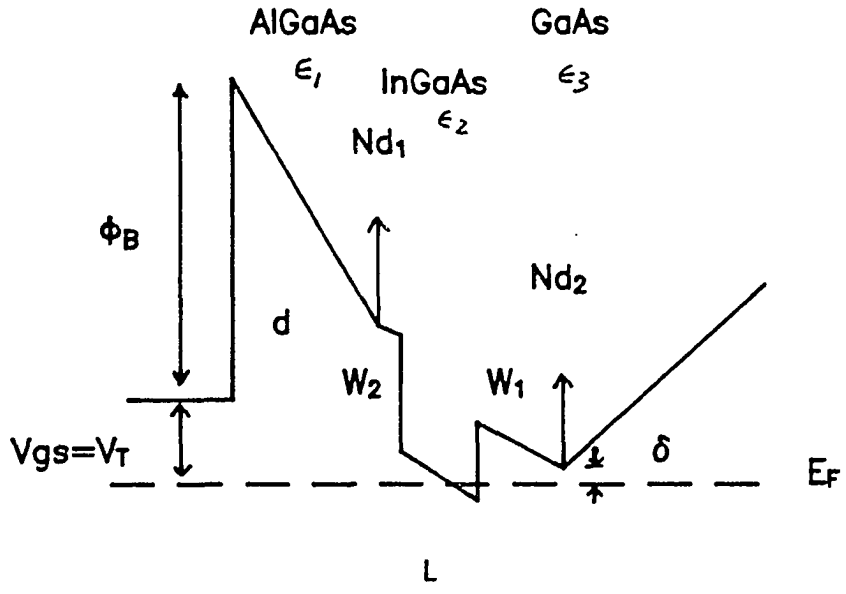

Figure 3.6. Conduction band diagram of the planar-doped quantum-well MODFET structure.

MODFET can be derived by solving a one-dimensional Poisson's equation with the help of the band diagram.

$$V_T = \Phi_B - [qN_{d1}d_1/\varepsilon_1 + (\varepsilon_3/\varepsilon_1(d_1+W_1) + \varepsilon_3/\varepsilon_2 L + W_2)qN_{d2}/\varepsilon_3] \quad (3.1)$$

$$- (\delta + \Delta E_{c1} - \Delta E_{c2} + E_o)/q \quad (1)$$

where Φ_B is the Schottky barrier height and E_o is the ground state energy of 2DEG. N_{d1} and N_{d2} are the silicon sheet doping densities in the AlGaAs and GaAs layers. w_1 and w_2 are the corresponding spacer layer thickness. d_1 and L are the thickness for the undoped AlGaAs layer and the quantum well. ΔE_{c1} and ΔE_{c2} are the discontinuities of the conduction bands, and δ is the difference of the doped GaAs conduction band minimum and the Fermi energy. ε_1, ε_2, and ε_3 are the permittivities of AlGaAs, InGaAs and GaAs respectively. From this equation, V_T is a linear function of d_1 in this planar doped MODFET structure in comparison with the conventional square rule dependence of the uniformly doped structures.

3.5. Microwave Performance

Microwave measurements have been performed from 0.5 to 26.5 GHz in 0.5 GHz steps with a pair of Cascade Microtech's microwave wafer probes and an HP8510 automatic network analyzer. S-parameter data have been taken with the gate and drain biased at various voltages, and fitted to the equivalent circuit model depicted in Fig. 3.7 through a computer optimization program FET-FITTER. Good agreements between the measured and modeled S-parameters

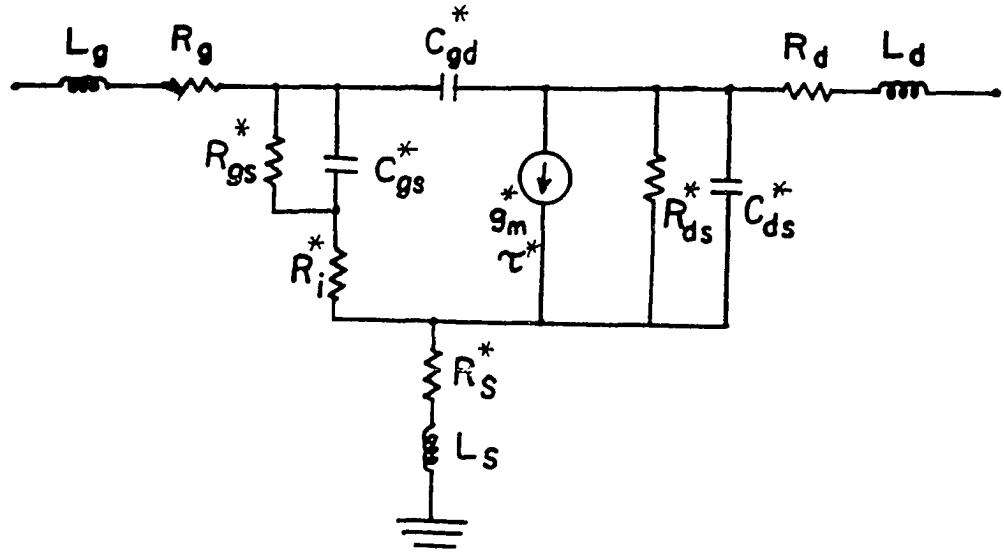

Figure 3.7. Non-linear MODFET equivalent circuit model.

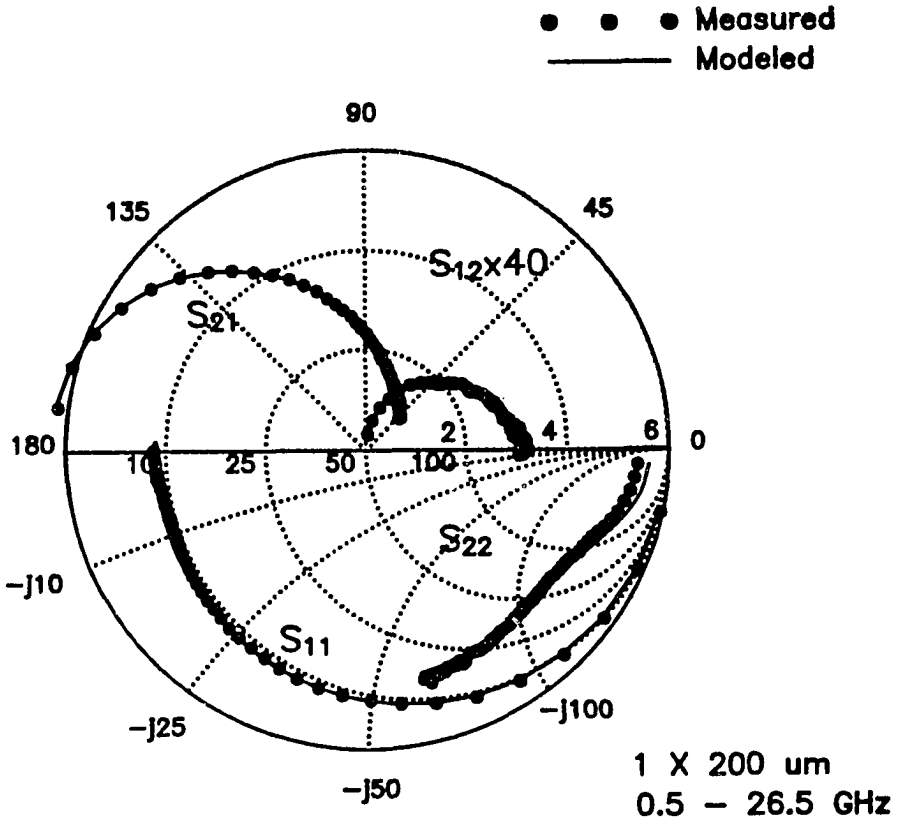

Figure 3.8. Measured and modeled S-parameters of a 1-μm MODFET.

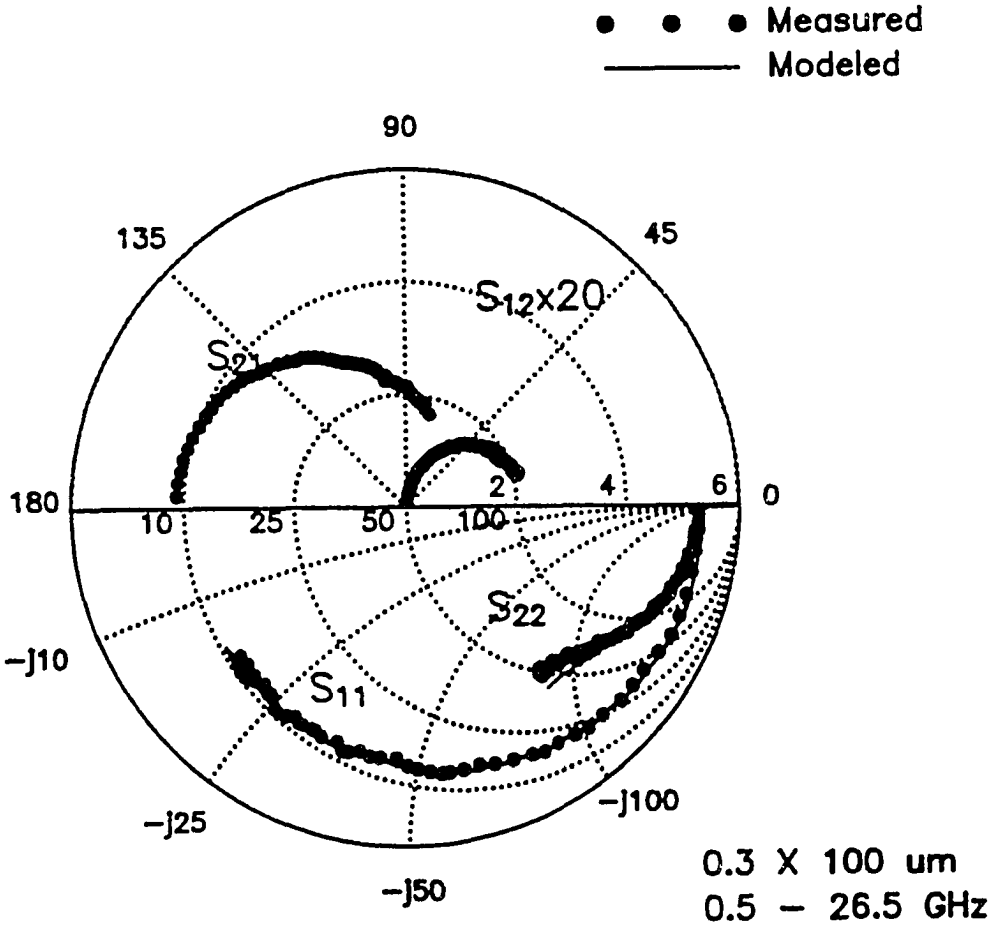

Figure 3.9. Measured and modeled S-parameters of a 0.3-μm MODFET.

of a 1 X 200 μm MODFET are shown in Fig. 3.8. The measured and modeled S-parameters of the 0.3 X 100 μm device is shown in Fig. 3.9 with an f_T of 45 GHz and an f_{max} of 120 GHz. The excellent DC and microwave performances are the results of good charge control and good carrier confinement through the planar-doped quantum well structure.

3.6. Bias-Dependent Equivalent Circuit Model

In order to investigate the nonlinear behaviors of the double heterojunction MODFET for large-signal applications, the elements of the equivalent circuit have to be examined closely for their bias dependence [13]. The measured S-parameters of the 1 X 200 μm MODFET at various gate and drain biases are used to determine the bias-dependent equivalent circuit parameters. All these S-parameter measurements are performed while the MODFET is biased in the current saturation region. The external device parasitics such as L_g, R_g, L_d, R_d, L_s, and R_s are assumed to be linear and invariant to the biases. The bias dependence circuit elements, which are marked with a '*' in Fig. 3.7 including g_m, C_{gs}, C_{ds}, C_{gd}, R_{ds}, R_{in}, and τ, are depicted in Figures 3.10-3.15.

As indicated by the charge control model in Chapter 2, g_m increases with V_{gs} initially and then is saturated once the parasitic AlGaAs channel is induced by a high gate bias. Because of the high aspect ratio (ratio of the gate length to the thickness of active layer) of MODFETs [14], the bias dependence of g_m in Fig. 3.10 shows less sensitivity to the V_{ds} variation. However, g_m decreases as

V_{ds} increases at positive gate bias. This deterioration of g_m is caused by the real-space transfer of hot electrons from the quantum well into the AlGaAs layer [15],[16], and will be discussed in Chapter 5.

For a given drain voltage, C_{gs} increases monotonically with increasing V_{gs}, as shown in Figure 3.11. The influence of V_{gs} on C_{gs} can not be fully explained by the basic charge-control theory of 2DEG [1]. The stronger dependence of C_{gs} on V_{gs} is possibly due to additional charge modulation in the AlGaAs layer [17]. When the gate is biased above 0.2 V, the parallel conduction in the AlGaAs layer starts and V_{gs} only modulates the charges in AlGaAs layer [18]. The slight increase of C_{gs} with increasing V_{ds} is therefore due to the increase of the depletion region between gate and drain as in the case of GaAs MESFET [13].

C_{ds} is dominated by the parasitic capacitance from drain to source through the active layers and the substrate, and is much less sensitive to the changes of the gate and drain biases (Figure 3.12). Similar bias dependence of C_{ds} was also found in the MESFET structures [13]. The capacitive coupling (C_{gd}) between gate and drain is through the gate fringing field. C_{gd} is reduced as the gate depletion region penetrates toward the drain with increasing potential difference, as shown in Figure 3.13.

The values of R_{ds} shown in Figure 3.14 are very high due to the excellent carrier confinement through the quantum well structure. This kind of

confinement is very essential for the high frequency performance of devices with short gate length. The increase of R_{ds} with increasing V_{ds} is caused by the extended depletion region between gate and drain. Nevertheless, the increasing gate current due to real-space-transfer hot electrons comes into play when V_{gs} is above 0.2 V, and R_{ds} shows abnormal behaviors.

τ represents the carrier transit time effect under the gate. As effective gate length is determined by the depletion region, the bias dependence of τ in Figure 3.15 is due to the variation of depletion region controlled by $|V_{ds}-V_{gs}|$.

3.7. Bias-dependent f_T and f_{MAG}

Fig. 3.16 and 3.17 show the bias-dependent f_T's and f_{max}'s of the 1 X 200 μm MODFET, calculated by using [19]

$$f_T = \frac{g_m}{2\pi C_{gs}}, \tag{3.2}$$

and

$$f_{max} = \frac{f_T}{[4(R_{in}+R_s+R_G)/R_{ds} + 4\pi f_T C_{gd}(R_{in}+R_s+R_G)]^{1/2}}, \tag{3.3}$$

because the stability factor (k) may not be greater than unity over the whole measured frequency for certain bias points. The 1-μm device is biased at V_{gs}= 0.6V and V_{ds}= 2V for a maximum f_T of 22GHz. The maximum f_{max} of 85GHz is obtained at V_{gs}=0.6V and V_{ds}=4V. This is the highest reported f_{max} for either GaAs MESFETs or MODFETs with 1-μm gate length. The drain voltage for the maximum f_{max} is higher than that for the maximum f_T because of higher R_{ds} and

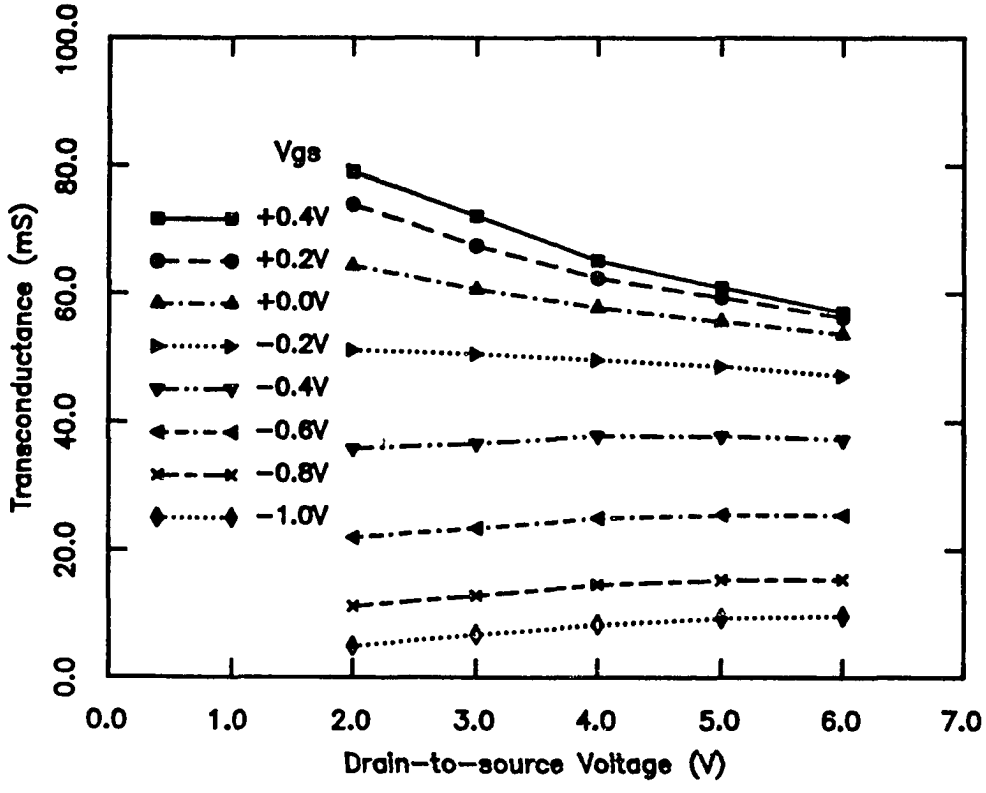

Figure 3.10. Transconductance (g_m) versus gate and drain bias.

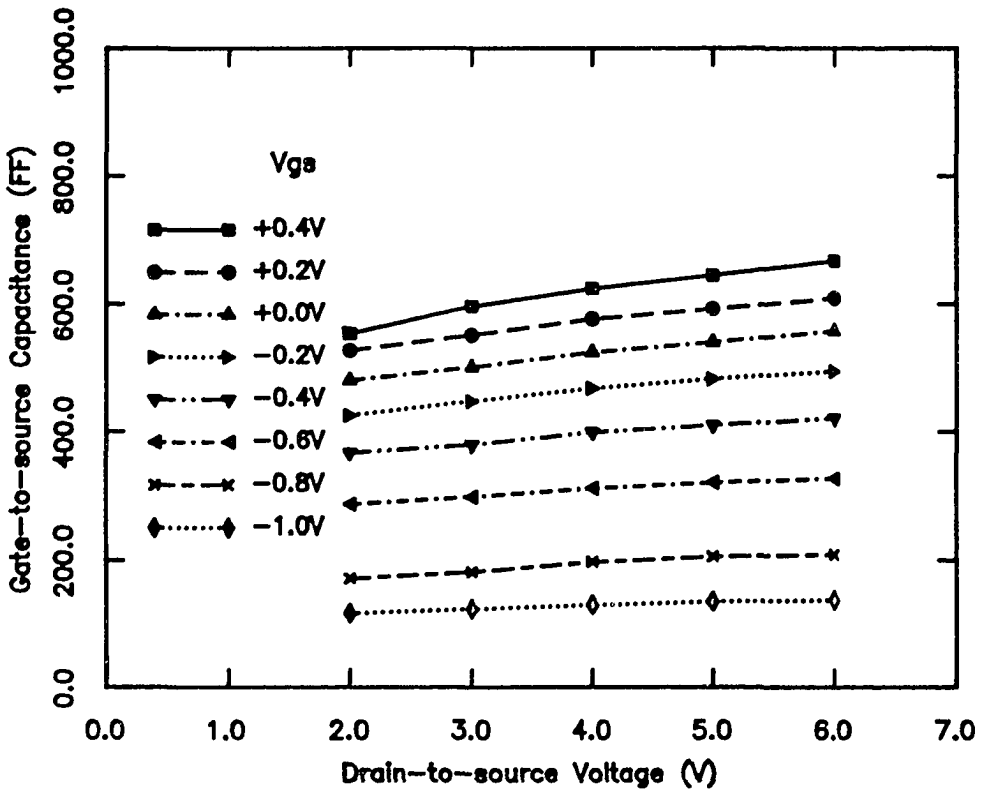

Figure 3.11. Gate-to-source capacitance (C_{gs}) versus gate and drain bias.

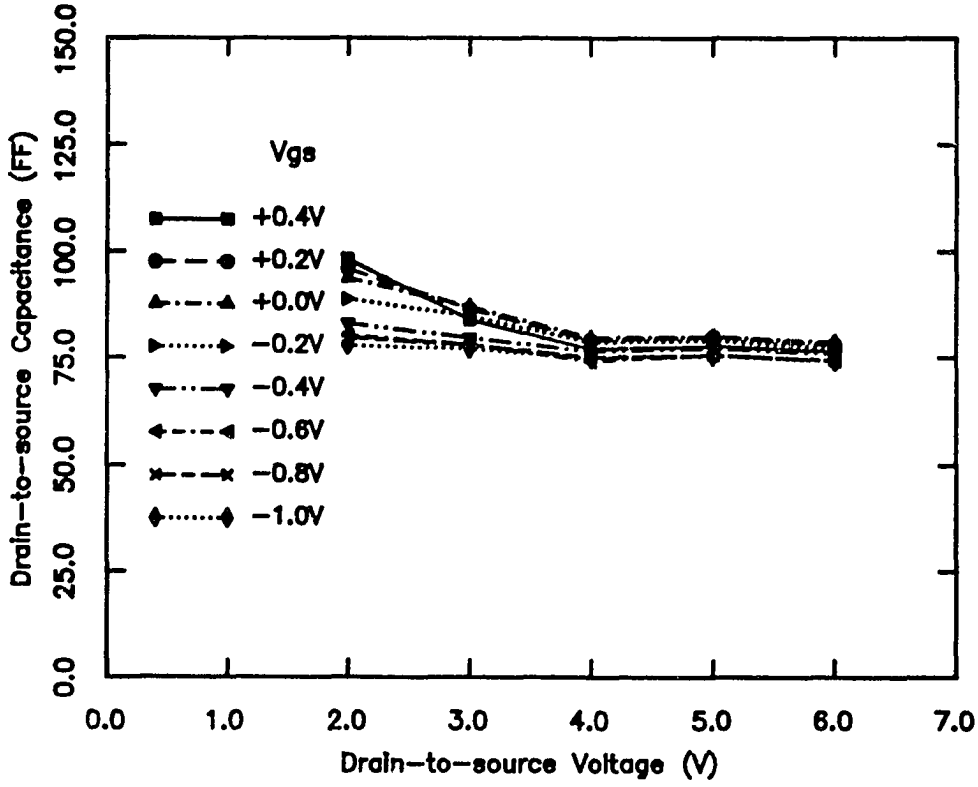

Figure 3.12. Drain-to-source capacitance (C_{ds}) versus gate and drain bias.

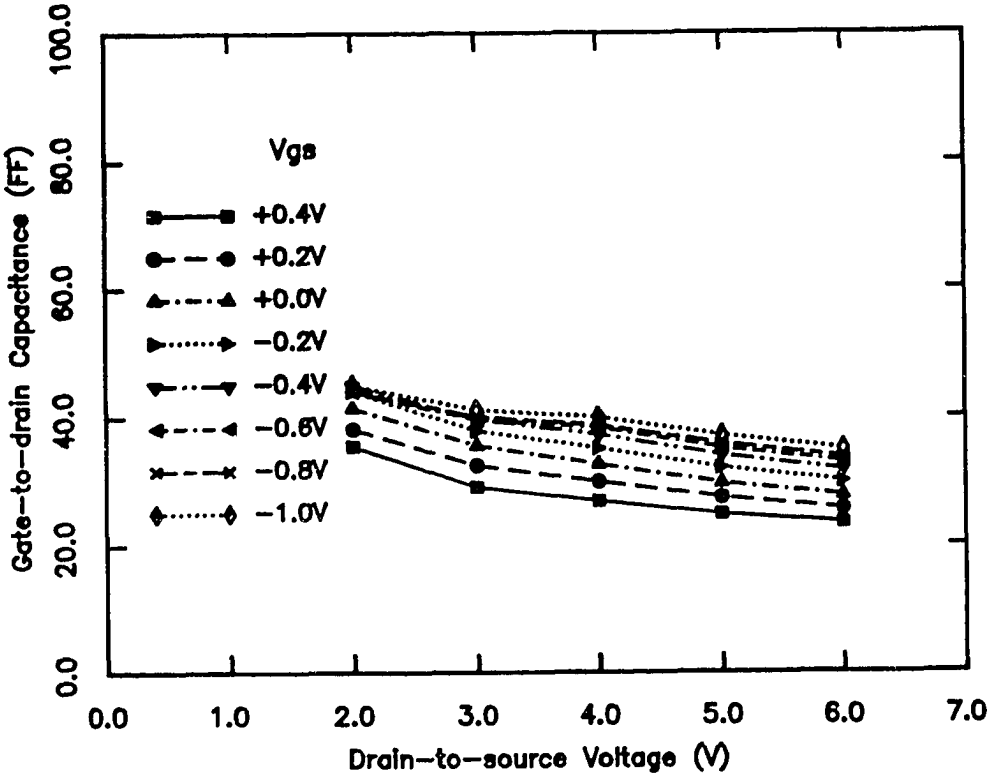

Figure 3.13. Gate-to-drain capacitance (C_{gd}) versus gate and drain bias.

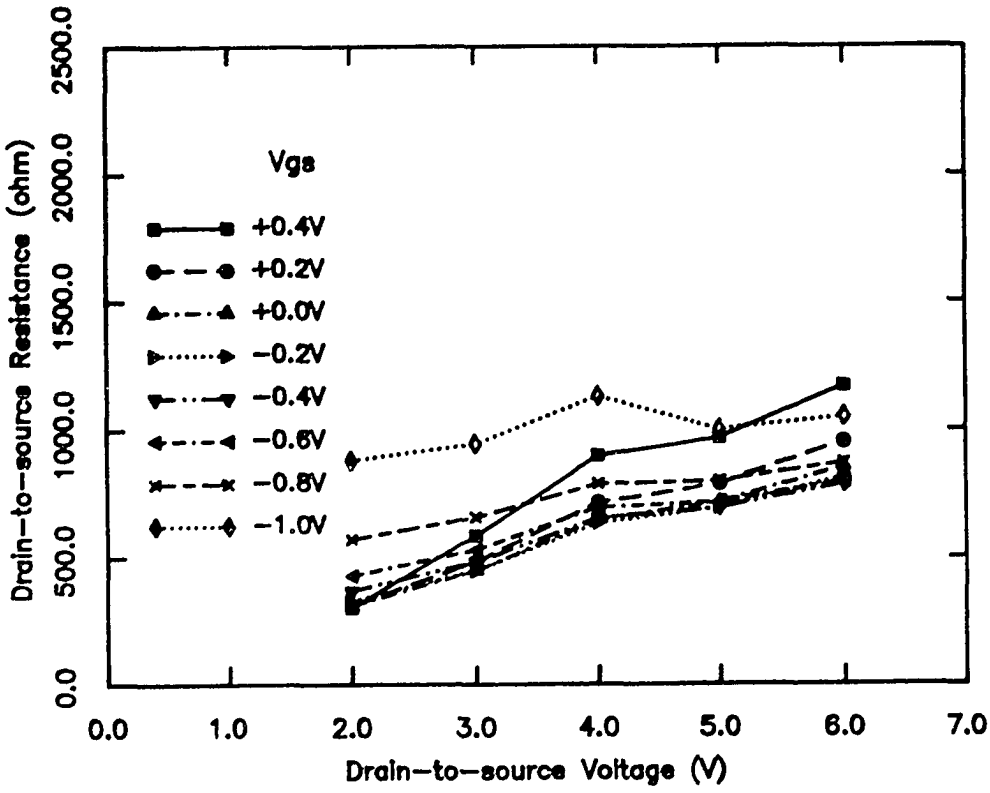

Figure 3.14. Output resistance (R_{ds}) versus gate and drain bias.

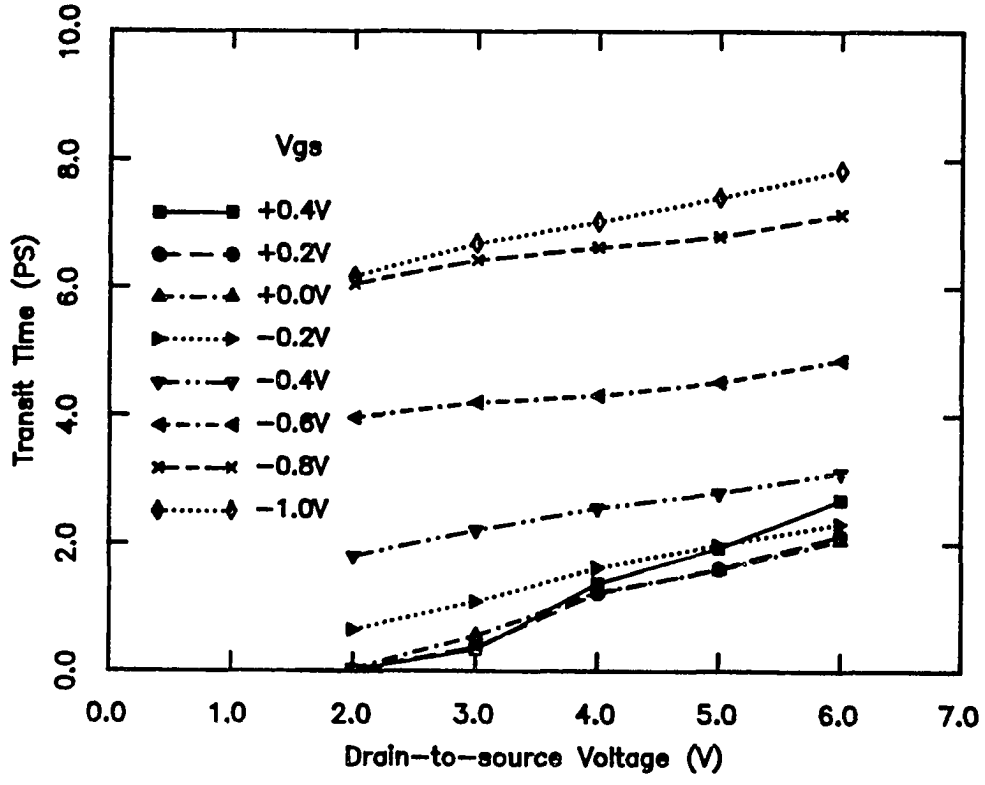

Figure 3.15. Transit time (τ) versus gate and drain bias.

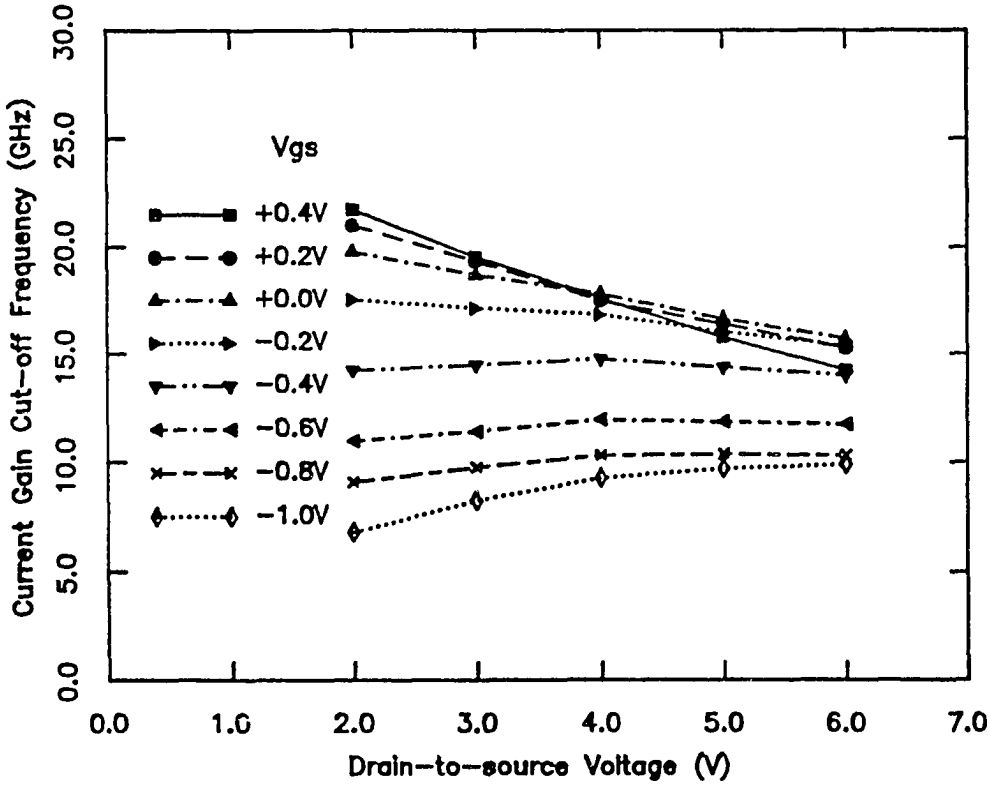

Figure 3.16. Current gain cut-off frequency (f_T) at various bias points.

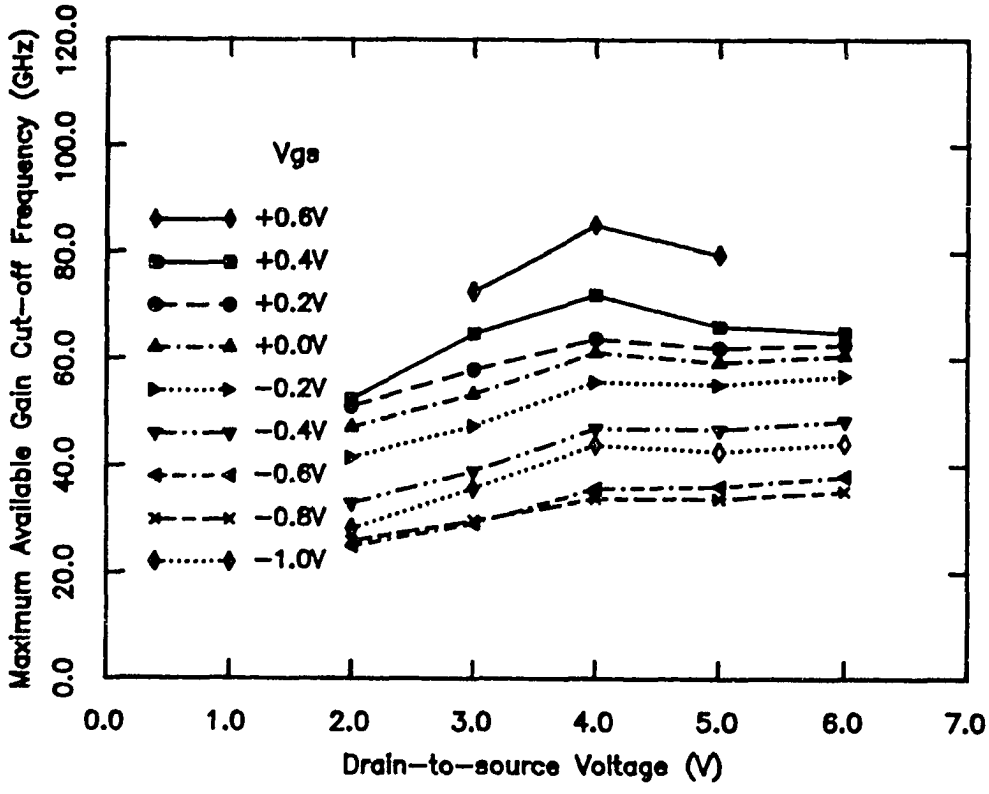

Figure 3.17. Maximum available gain cut-off frequency (f_{MAG}) at various bias points.

lower C_{gd} from the wider AlGaAs depletion region between gate and drain.

3.8. Summary

AlGaAs/InGaAs/GaAs double heterojunction MODFETs with 1-μm and 0.3-μm gate length have been fabricated and characterized at DC and microwave frequencies. Excellent microwave performance has been achieved with an f_T of 22 GHz and an f_{max} of 85 GHz from the 1-μm device, and an f_T of 45 GHz and an f_{max} of 120 GHz from the 0.3-μm device.

Bias-dependent equivalent circuit models have been determined to study the nonlinear behavior of the 1-μm device under large-signal conditions. In general, the bias-dependent circuit parameters of MODFETs behave quite similar to that of GaAs MESFETs. Distinctive features of MODFETs, such as the heterojunction charge control, AlGaAs parallel conduction, quantum well carrier confinement, and real space transfer, make the bias-dependence of circuit parameters more complicated. This study will be helpful to understand the device physics and to optimize MODFET structures. It also provides valuable information to construct the large-signal model for computer-aided design and simulation of nonlinear microwave and high-speed digital MODFET integrated circuits.

3.9. References

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CHAPTER 4

REDUCTION OF SHORT-CHANNEL EFFECTS

4.1. Introduction

Modulation-Doped Field-Effect Transistors (MODFETs) have shown rapid progress in the microwave and digital applications [1,2]. Reported current densities of single-heterojunction GaAs/AlGaAs or pseudomorphic InGaAs/AlGaAs are around 200 mA/mm, limited by the available two-dimensional electron gas (2DEG) sheet charge density (typically less than $1.0 \times 10^{12} cm^{-2}$). High current driving capability is essential to reduce the propagation delay in the high speed digital circuits and to increase the power density of the microwave amplifiers. In additional to developing new material systems, such as GaInAs/AlInAs on InP [3,4], for larger conduction-band discontinuity and better electronic transport properties, multiple heterojunction MODFETs based on the GaAs/AlGaAs system have been investigated [5-7]. Current density as high as 450 mA/mm from a pseudomorphic DH-MODFET [8] and 1070 mA/mm from a pseudomorphic double quantum-well MODFET [9] have been reported with excellent microwave performance.

Despite the high current density and high current gain cut-off frequency (f_T) achieved by these devices, the maximum available power gain cut-off frequency

(f_{MAG}) of DH-MODFETs, which dictates the usable frequency limit of high speed devices, were not much higher than those obtained from the single heterojunction devices. Besides, the bottom inverted heterojunctions from the previous structures were not contributing as many two-dimensional electrons as their corresponding top heterojunctions due to the low doping densities in the bottom electron supplying layers. Low doping densities along with tight controls of the thickness of the bottom spacer layer are necessary to deplete the n-type bottom electron supplying layer totally such that no parasitic conduction occurs during FET operation [10]. Moreover, this bottom parasitic conduction will be enhanced by the FET bias as the real-space transferred hot 2DEG electrons are injected into the buffer and bottom supply layer with the high drain electric field [11,12]. Once the parasitic conduction channel is built up in the low-mobility bottom electron supply layers, poor FET pinch-off characteristics and high output conductance are resulted. These lead to inferior FET performance such as low available power gain, poor power-added efficiency, and high harmonic distortions for microwave applications. Large sub-threshold current will also deteriorate the noise margin of the digital integrated circuits and increase the power consumption.

High electron-barrier buffer layers, such as AlGaAs, superlattice, and buried p^+-GaAs layers have been studied extensively for GaAs MESFETs [13-15] to improve the FET power saturation characteristics and to reduce the

undesired short channel effects. In this work, n^+-GaAs/InGaAs/n^+-AlGaAs double heterojunction MODFET structures with superlattice buffer layers and buried p^+-GaAs layers are studied. DH-MODFETs with 1.2-μm and 0.3-μm gate length are fabricated and characterized at DC and microwave frequency. Two major advantages by using high electron barrier buffer layers are observed. First, the bottom electron supply layer can be doped much heavier and hence generate more two-dimensional electrons before the onset of a parasitic conducting channel. Second, the high barrier buffer layers further reduce the real-space transfer of hot two-dimensional electrons deeply into the buffer with the high drain bias. As a result, high FET channel current and large RF gain can be achieved simultaneously.

4.2. Layer Structures

The DH-MODFET structures are grown by MBE on semi-insulating GaAs substrates. As depicted in Fig. 4.1, three DH-MODFET structures are prepared with identical top layers but different buffer layer structures. Either an AlGaAs/GaAs superlattice or a buried beryllium-doped p^+-GaAs layer is utilized as the high electron potential barrier buffer layer. A reference layer with an undoped GaAs buffer is also grown for comparison. The conduction band diagrams of these DH-MODFET structures are shown in Fig. 4.2. The active channels use lattice-strained InGaAs quantum well for its superior electronic transport properties [16]. The bottom electron supply layer employs a silicon

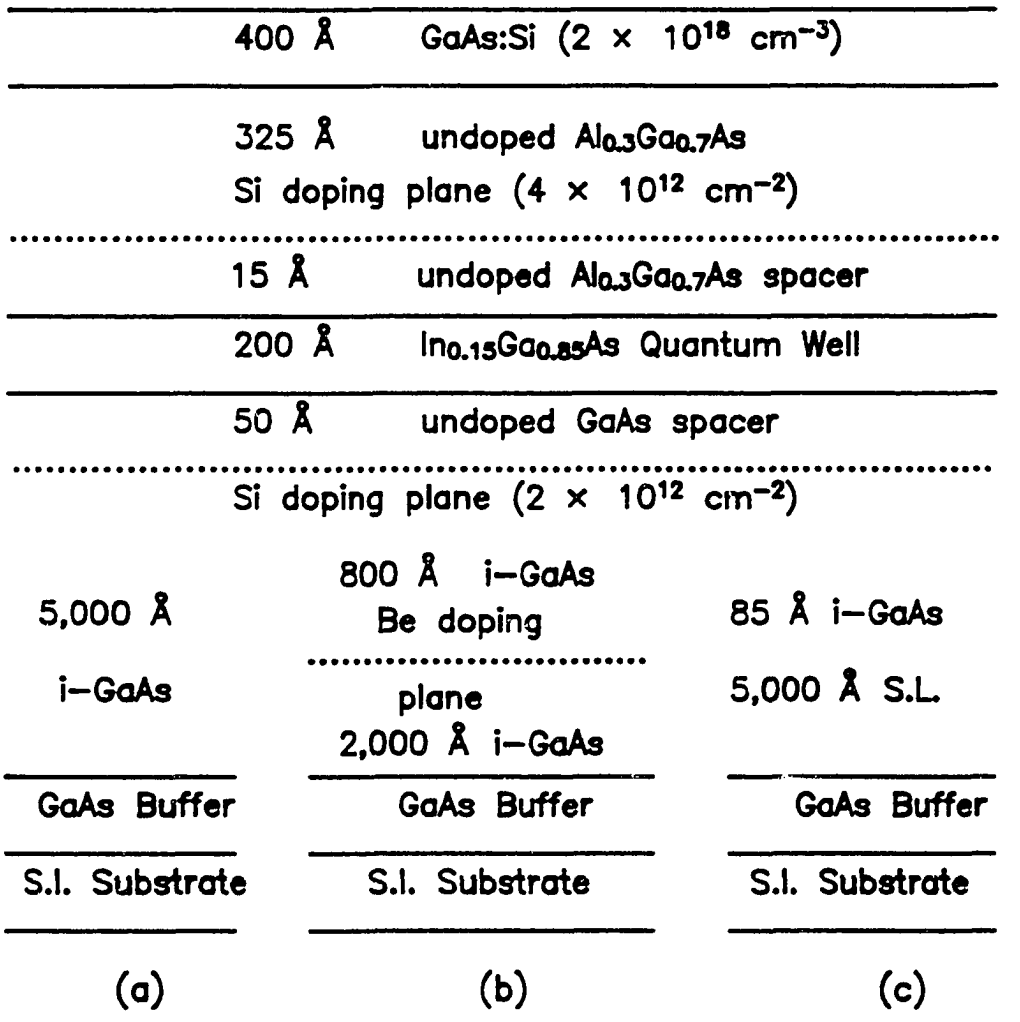

Figure 4.1. DH-MODFET structures with the same channel and top layers but different buffers: (a) i-GaAs, (b)p^+-GaAs, (c)superlattice.

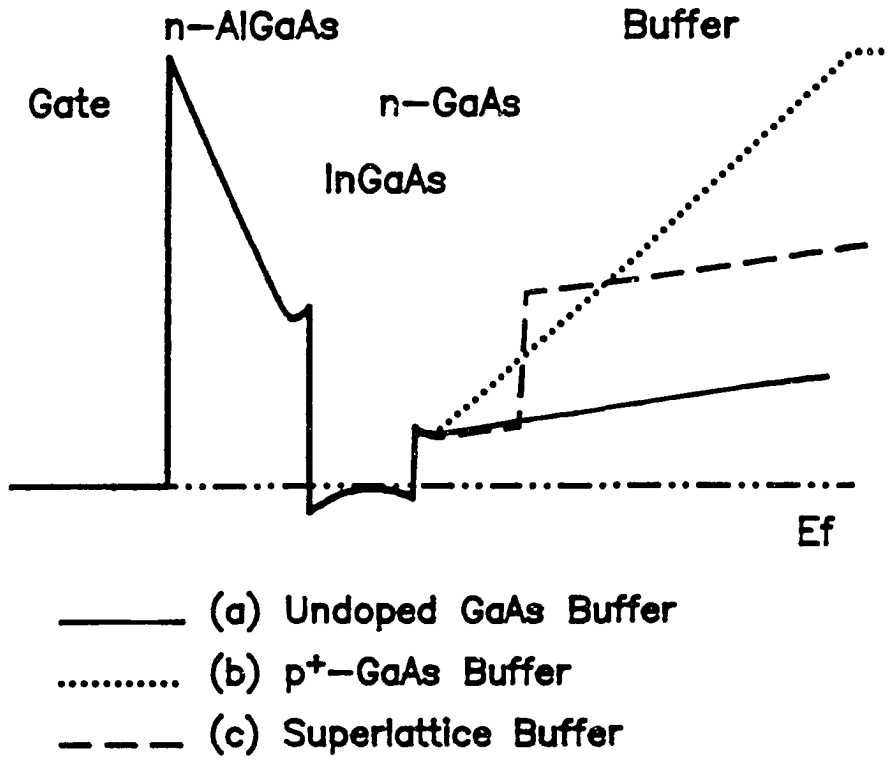

Figure 4.2. Conduction band diagrams of DH-MODFET structures with un-doped GaAs, p^+-GaAs, and superlattice buffer.

planar-doped GaAs layer to circumvent the difficulty in obtaining high quality heterointerface when the GaAs layer is grown on top of AlGaAs layer [17-21] at a elevated growth temperature for high quality AlGaAs layer [18]. The lower growth temperature (typically 530-560 C) for InGaAs and GaAs layers further reduces the segregation of silicon dopants [20,21] from the bottom electron supply layer and beryllium dopants from the buried p^+-GaAs buffer layer into the InGaAs channel [22].

The mole fractions of aluminum and indium are 30% and 15% throughout the layers. All the dopants are placed in very thin layers by introducing the silicon or beryllium dopants during the MBE growth interruptions. This planar doping technique has been proven to be very effective in reducing the low temperature light sensitivity, improving the transconductance and aspect ratio, and increasing the breakdown voltage in the heterojunction MODFET structures [23].The silicon sheet doping densities are $6x10^{12}$ cm^{-2} and $2x10^{12}$ cm^{-2} in the top and bottom supply layers respectively. The beryllium doping density is kept low ($5x10^{11}$ cm^{-2}) to ensure that the p^+-GaAs buffer layer is totally depleted under any FET biases to avoid possible parasitic hole conduction and parasitic gate capacitance.

The grown wafers were then fabricated with a conventional recess-gate FET process as outlined in Chapter 3. Typical contact resistance (Rc) is 0.04 ohm-mm obtained from transmission line measurements. The gate pattern is

defined either by mid-UV contact lithography for 1.2-μm gate length or by electron beam lithography for 0.3-μm T-shape gate. The gate resistance is typically 120 ohm/mm from DC end-to-end measurement and verified by microwave S-parameters [24]. This low gate resistance improves the power gain at high frequency.

4.3. Parasitic Charges at Thermal Equilibrium

From a one-dimensional classical electrostatic computer model [25], the 2DEG sheet charge densities and the free electron density in the bottom electron supply layer of the DH-MODFET structures, without the presence of a drain bias, can be calculated for various gate biases. For the same amount of 2DEG density, the high electron barrier buffer reduces the number of free electrons in the bottom supply layers, as shown in Fig. 4.3. On the other hand, when the doping density in the bottom supply layer increases, more 2DEG can be accumulated in the quantum well by the high barrier buffer without increasing the parasitic electrons. The maximum 2DEG density contributed from the inverted heterointerface is limited by the heterojunction discontinuity, etc. [26]. From the simulation, an additional 2DEG density of 2.5×10^{11} cm^{-2} could be obtained in a DH-MODFET with p^+-GaAs buffer layer compared to a DH-MODFET with undoped GaAs buffer layer with the same amount of parasitic free electrons, as depicted in Fig. 4.4.

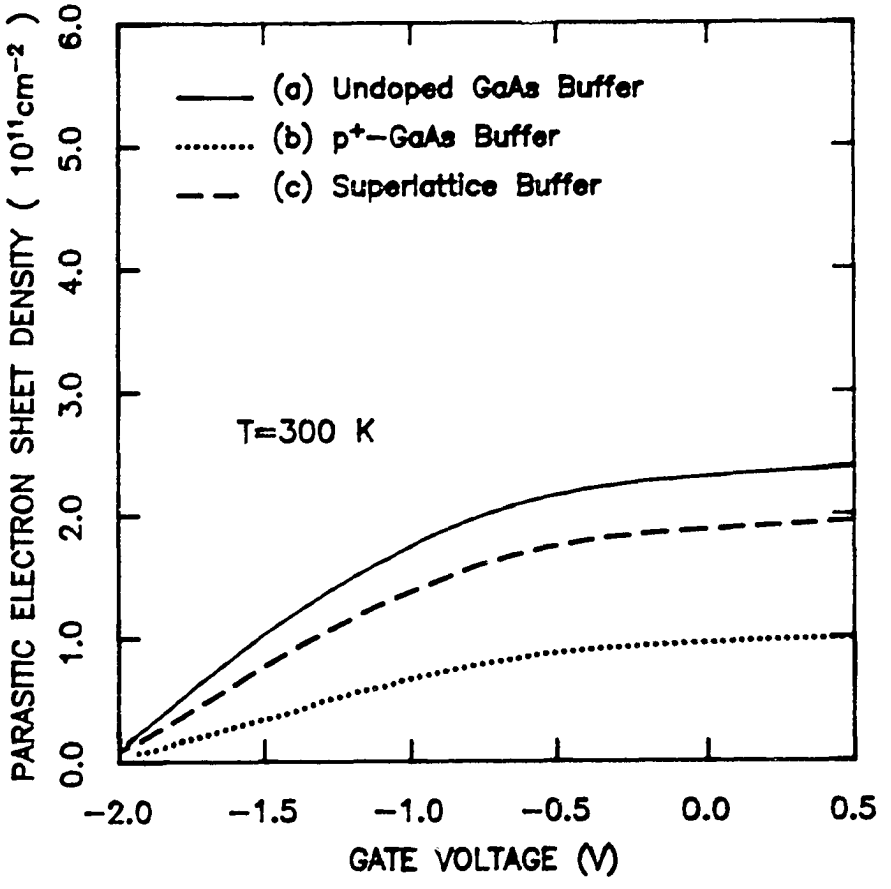

Figure 4.3. Parasitic electron densities vs. V_G for various buffers with the same amount of 2DEG density in the quantum-well.

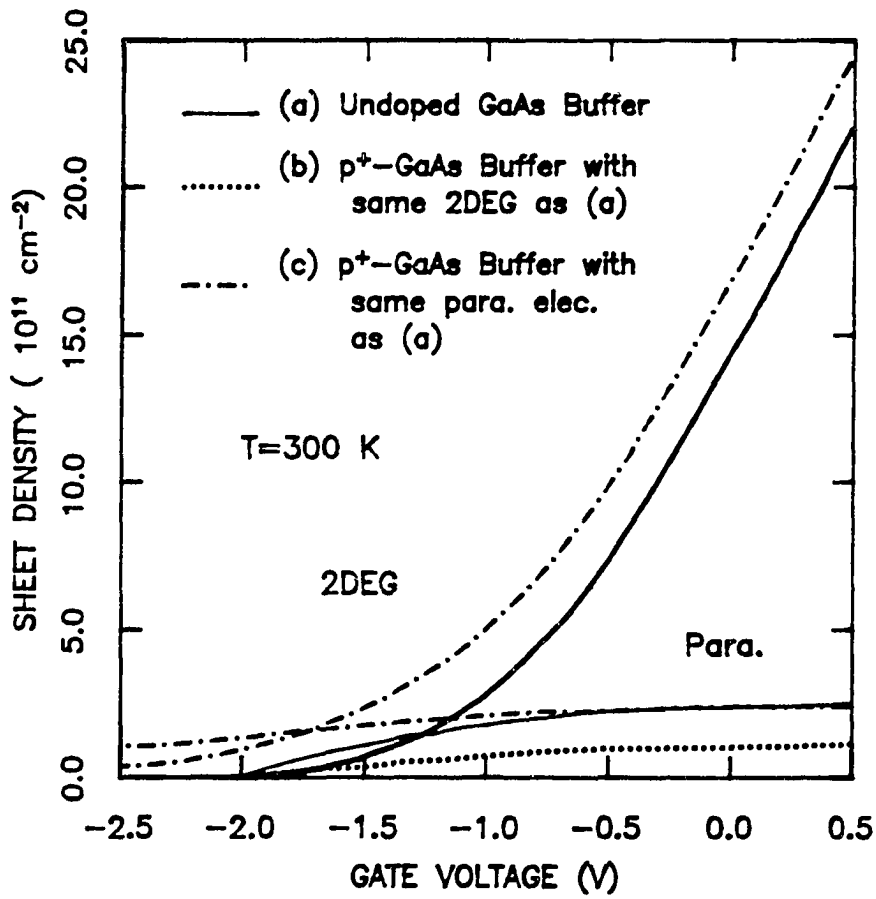

Figure 4.4. 2DEG density in the quantum-well vs. V_G for various buffers with the same amount of parasitic electrons in the buffer.

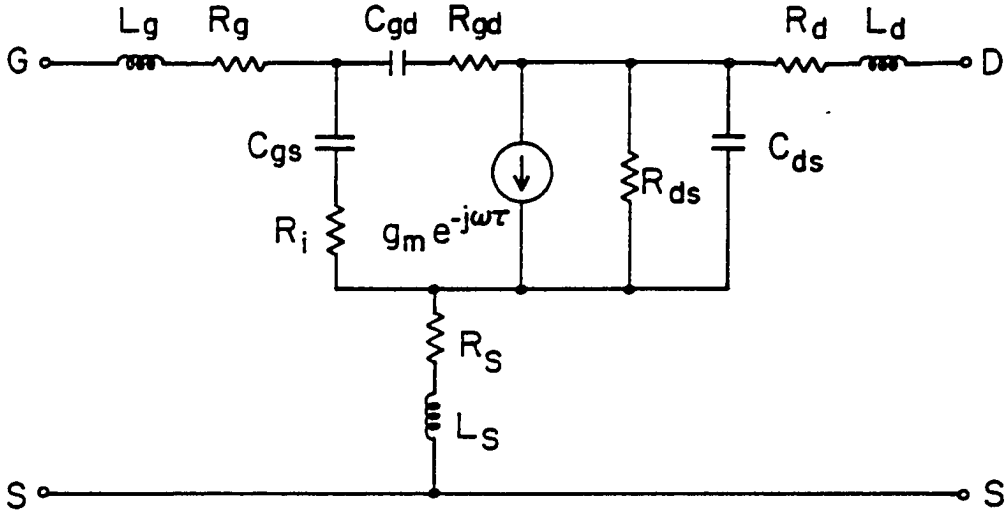

Figure 4.5. Small-signal equivalent circuit model of DH-MODFETs.

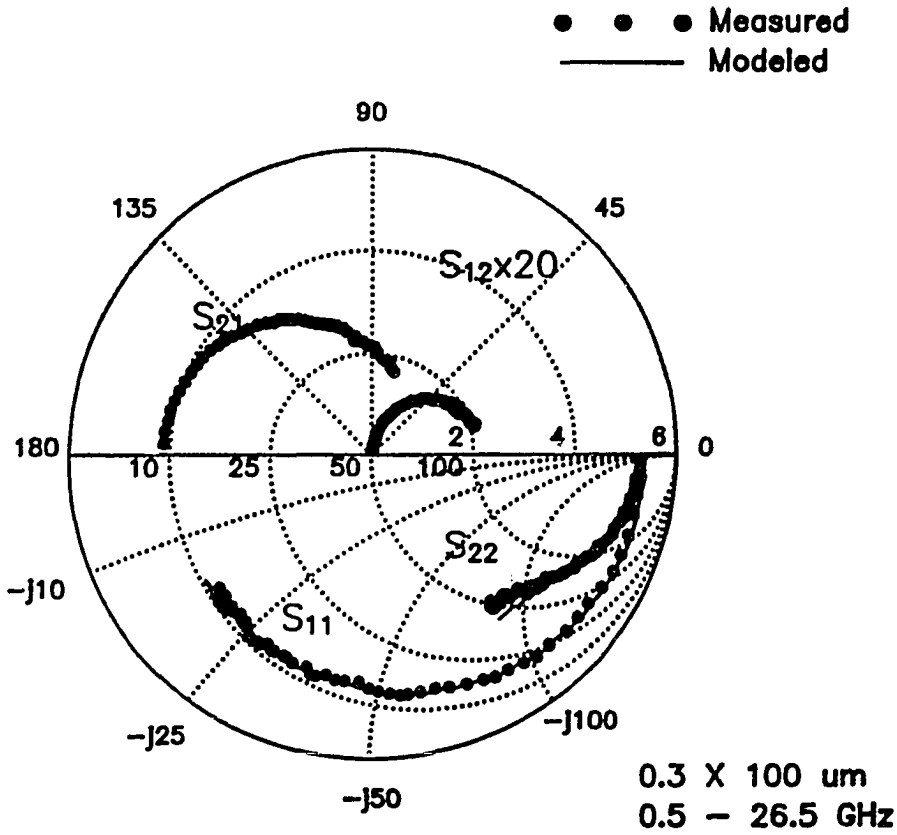

Figure 4.6. Measured and modeled S-parameters of a 0.3x100 μm DH-MODFET.

However, this 1-D simulation is performed at the thermal equilibrium in the absence of the applied drain potential. Under a real FET operation, some of two-dimensional electrons in the channel will acquire enough energy from the high drain field to be transferred in the real-space into the supplying layers. This real-space transfer phenomenon [11] may lead to negative differential resistance and potential device instability, as will be discussed in Chap. 5. These parasitic carriers in the low-mobility wide bandgap electron supplying layers will generate substrate current and increase FET parasitics, which result in poor high frequency performance.

4.4. Experimental Results and Discussions

The fabricated devices are characterized at both DC and microwave frequencies. Microwave measurements are performed from 0.5 to 26.5 GHz on the wafer with a pair of microwave wafer probes and an HP8510 automatic network analyzer. The influence of different buffer layers on the full channel current, transconductance and two-dimensional electron sheet charge densities can be examined by DC I-V and C-V measurements. From the microwave S-parameter measurements, various figures-of-merit such as f_T and f_{MAG}, can be extracted. The measured data are further fitted into the equivalent circuit model as shown in Fig. 4.5 with a microwave CAD program such as Super-Compact. Typical measured and modeled S-parameters are shown in Fig. 4.6 for a 0.3X100 μm DH-MODFET with superlattic buffer. The root-mean-square errors of fitting are

generally less than 3.5 % over the whole frequency range. The normalized value of equivalent circuit elements are tabulated in Table 4.1 for DH-MODFETs with different gate length and buffer configurations.

Despite the possible small processing variations (such as recess etch depth) among different wafers, the DC and microwave data provide us with rich information in understanding the device behavior under the influence of different buffer layer configurations. Table 4.2 summarizes the device performance of 1.2-μm and 0.3-μm gate DH-MODEFTs for different buffer configurations. Detailed discussions on the buffer effects are provided in the following paragraphs.

4.4.1. GaAs buffer

Fig. 4.7 shows the drain current-voltage characteristics of a MODFET with 1.2 X 100 μm gate geometry at room temperature. Despite the high full channel current of 550 mA/mm and high peak DC transconductance (g_m) of 366 mS/mm, this DH-MODFET shows a very poor pinch-off characteristics because of the parallel conduction in the bottom GaAs supply layer. This large parasitic current, which can not be modulated by the gate signal, results in a low f_T of 11.5 GHz and f_{MAG} of 20 GHz. The pinch-off characteristics of the DH-MODFET with a 0.3-μm gate length is also very poor.

Table 4.1 Normalized equivalent circuit parameters for DH-MODFETs with different buffers.

Wg=100um		Lg= 1.2 um		0.3 um	
Buffer Type		p^+–GaAs	S.I.	p^+–GaAs	S.I.
Vgs	(V)	0.2	0.4	0.6	0.6
Vds	(V)	2.5	2.5	3.5	2.5
Rg	(Ω)	11.2	8.54	1.08	1.97
Ri	(Ω)	4.4	3.82	4.39	3.98
Rs	(Ω)	6.22	3.40	5.02	1.84
Rd	(Ω)	25.00	19.06	9.22	3.81
$g_{ds}(R_{ds}^{-1})$	(mS)	0.212	0.267	0.126	1.570
Cgs	(fF)	268.6	319.9	188.1	196.6
Cds	(fF)	23.99	42.31	24.36	28.26
Cgd	(fF)	6.43	12.43	6.77	10.59
g_m	(mS)	28.42	42.42	40.44	52.33
τ	(ps)	1.80	1.02	1.80	0.78

Table 4.2 Comparison of device performance for DH-MODFETs with different buffers.

Gate Length	Lg = 1.2 um			Lg = 0.3 um		
Buffer Type	GaAs	P^+–GaAs	S.L.	GaAs	P^+–GaAs	S.L.
Pinch–off	poor	good	good	poor	good	fair
Idss (mA/mm)	550	470	620	–	480	720
gm ext (mS/mm)	366	382	410	–	372	450
f_T (GHz)	11.5	16.5	21.5	–	40	45
f_{MAX} (GHz)	20.0	76.0	80.0	–	180	120
$\langle n_s \rangle$ (77K,C–V) (cm^{-2})	–	3.2 E12	2.3 E12	–	–	–
$\langle n_s \rangle$ (300K,f_T) (cm^{-2})	–	1.8 E12	1.5 E12	–	–	–

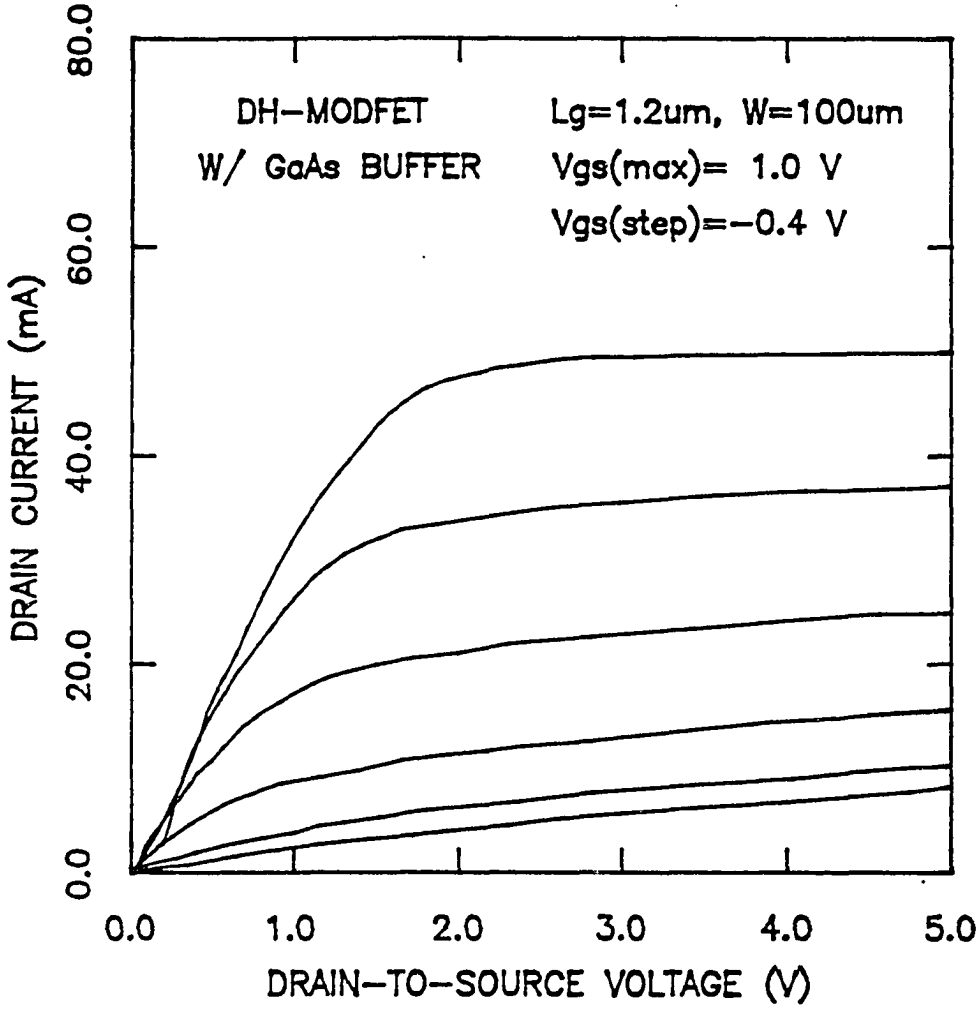

Figure 4.7. I-V characteristics of a 1.2x100 μm DH-MODFET with an undoped GaAs buffer layer.

4.4.2. Superlattice Buffer

AlGaAs/GaAs superlattice buffer layer is known to getter the out-diffused impurities from the substrate [17, 19]. The mobilities of the heterointerface grown on top of a superlattice buffer are enhanced [17], while the backgating transconductance [27] and the deep level traps in the grown GaAs epilayer can be reduced [14]. This results in better electronic transport properties which lead to the enhanced device performance such as higher current density, higher f_T and improved noise performance. The conduction band discontinuity at the GaAs/superlattice interface also acts as an energy barrier preventing the hot electron injection into the buffer layer under a high drain electric field. This barrier effect together with the reduced free electron density in the bottom supply layer, as simulated in the one-dimensional static heterojunction model, reduces the output conductance and buffer current. A full Monte Carlo simulation, such as described in [28], would provide more information on the hot electron confinement. However, the experimental results from fabricated DH-MODFETs does demonstrate the effectiveness of the superlattice buffer layer in confining 2DEG carriers and the improvement of channel quality.

Fig. 4.8 shows the DC drain I-V characteristics of a DH-MODFET with 1.2 X 100 μm gate geometry. The device demonstrates a full channel current of 620 mA/mm and a g_m of 410 mS/mm with a very good pinch-off characteristics. An f_T as high as 21.5 GHz and an f_{MAG} of 80 GHz have been extrapolated from

the measured s-parameters with a -6 dB/octave gain slope. There are some negative drain differential resistance (NDR) observed in the I-V characteristics at large forward gate bias. This is due to the removal of real-space transferred hot 2DEG in the top AlGaAs supply layer with a forward-biased gate electrode as reported in [29] and will be discussed in Chap. 5.

The DC I-V characteristics of a 0.3 X 100 μm DH-MODFET is shown in Fig. 4.9. The full channel current and g_m are 720 mA/mm and 450 mS/mm, which are about the same as the 1.2-um FETs. From the s-parameter measurements, f_T of 45 GHz and f_{MAG} of 120 GHz are obtained. Although these cut-off frequencies are very good for the DH-MODFETs, they are much less than what would be expected by scaling up the RF performance from these 1.2-μm FETs. There is a sign of short channel effect in the DC I-V characteristics such as slight g_m compression near FET pinch-off. It suggests that the electron barrier (approximately 0.24 eV) provided by $Al_{.3}Ga_{.7}As$/GaAs superlattice may not be high enough to reduce the hot electron injection into the buffer layers in 0.3-μm devices under a high drain field [30]. This is further verified by the RF output conductance (g_{ds}) in the equivalent circuit as listed in Table 1. g_{ds} is degraded from 2.67 mS/mm of a 1.2-μm device to 15.7 mS/mm of a 0.3-μm device. It is necessary to use higher energy barrier in short-channel MODFET devices to reduce the substrate current [31,32].

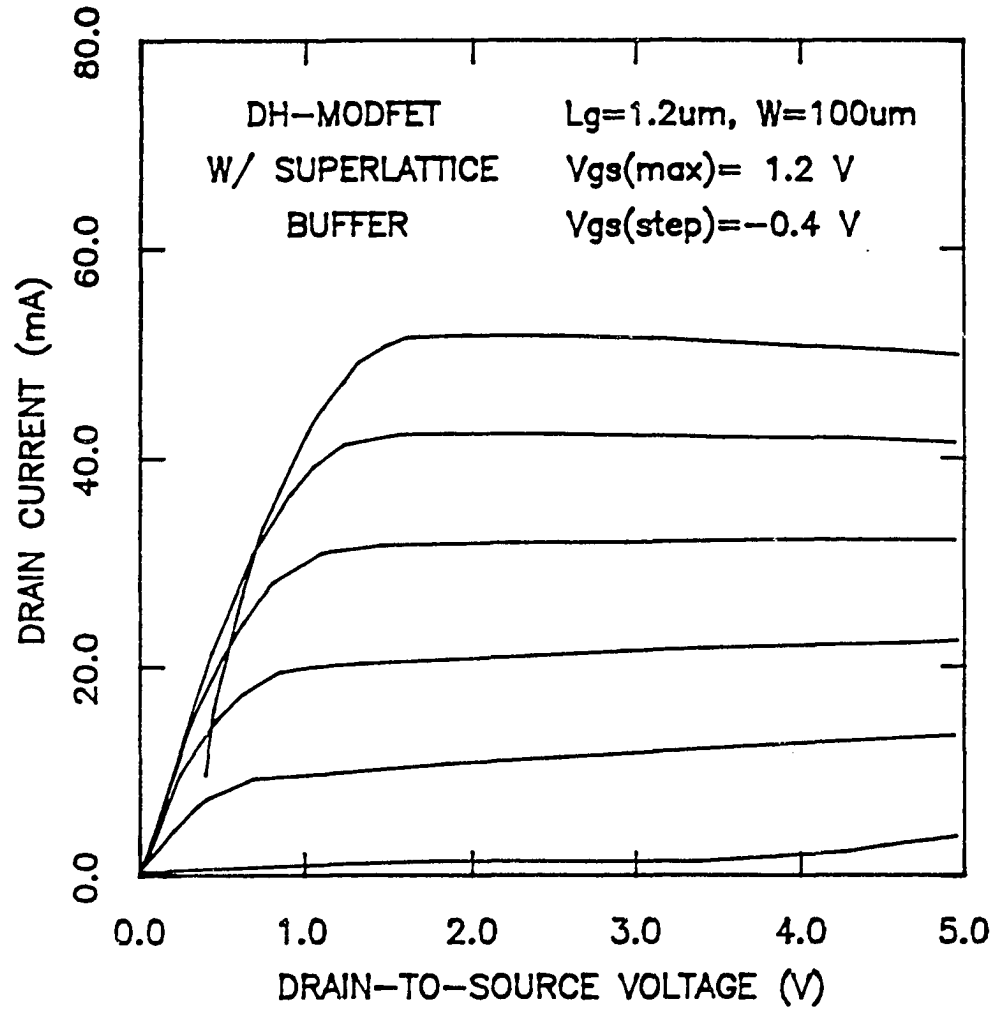

Figure 4.8. I-V characteristics of a 1.2x100 μm DH-MODFET with a superlattice buffer layer.

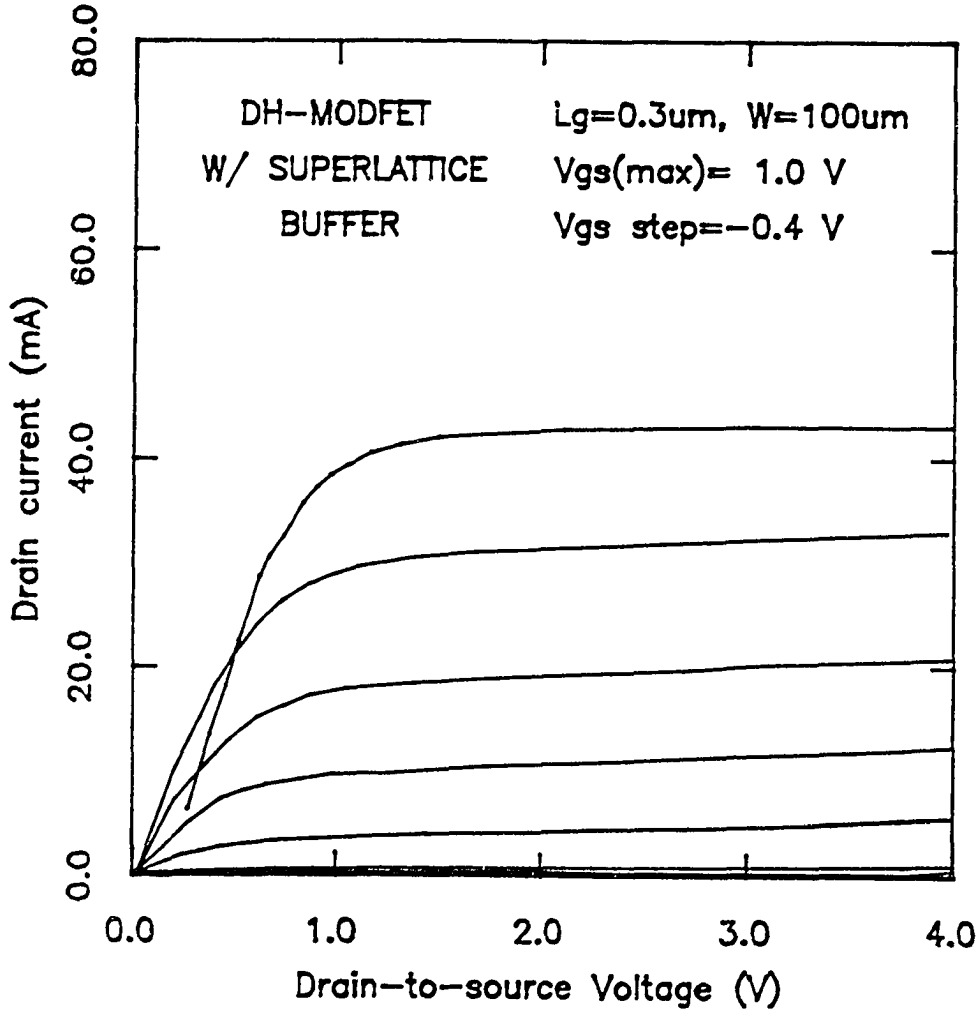

Figure 4.9. I-V characteristics of a 0.3x100 μm DH-MODFET with a superlattice buffer layer.

As suggested in [11] and experimentally observed in [12,29], the mechanism of real-space transfer of hot 2DEG out of quantum-well channel exists at both the top AlGaAs/InGaAs and bottom InGaAs/GaAs hetero-interfaces, so long as the 2DEG acquires enough energy to overcome the potential barrier. This carrier deconfinement mechanism reduces the available 2DEG in the high mobility channel, lower the current density, and deteriorates high frequency performance of the MODFETs.

4.4.3. Buried p^+-GaAs Buffer

Buried p^+-GaAs (BP) buffer layers have been found to be very effective in isolating the GaAs MESFET channel from the defects and impurities in the substrate. Compared to the conventional MESFETs, BP-MESFETs exhibit improved performance such as suppression of drain current transients [33], enhanced immunity to the ionizing optical radiation [34], reduced gate-drain breakdown current [35], reduction of backgating, and frequency-dependent dispersions of small-signal device characteristics [35]. Due to the reduction of sub-threshold current in BP-MESFETs, the uniformity of threshold voltages is maintained with improved output conductance when the gate length is reduced down to the submicron regime [36,37]. Digital propagation delays below 10 ps/gate [37] and high speed LSI circuits [38] have been demonstrated with a BP-SAINT GaAs MESFET technology.

Buried p-buffer layers have been investigated to improve the confinement 2DEG in the single-heterojunction MODFET [39] and the double-heterojunction MODFET structures [40]. Although the single-heterojunction MODFETs with buried p-GaAs buffer is suitable for the low-noise, low-power, and high gain applications, the available 2DEG density at heterointerface is reduced by the acceptors in the p-type buffer layer owing to the charge neutrality. Therefore, its current density will be reduced by the amount of p-type dopants introduced into the buffer layer. This problem can be avoided in the DH-MODFET with a buried p-type buffer layer by increasing the silicon doping density in the bottom supply layer to offset the p-type dopants in the buffer. As a result, a high electron energy barrier up to 0.7 eV can be established by the built-in electric field in the BP-buffer, and better carrier confinement is achieved.

The DC drain I-V characteristics of a 1.2 X 100 μm DH-MODFET is depicted in Fig. 4.10. The normalized full channel current and g_m are 472 mA/mm and 382 mS/mm. The 1.2-um device yields very good pinch-off characteristics as well as high f_{MAG} of 76 GHz despite a poor f_T of 16.5 GHz and lower drain current. f_T is deteriorated because of the possible out-diffusion of substrate impurities and rapid redistribution of p-type beryllium dopants through interstitial diffusion [22] into the quantum-well channel during the MBE growth. These effects are also verified by the 15 % reduction of the current density in these devices compared to those with superlattice buffer, while the effective donor

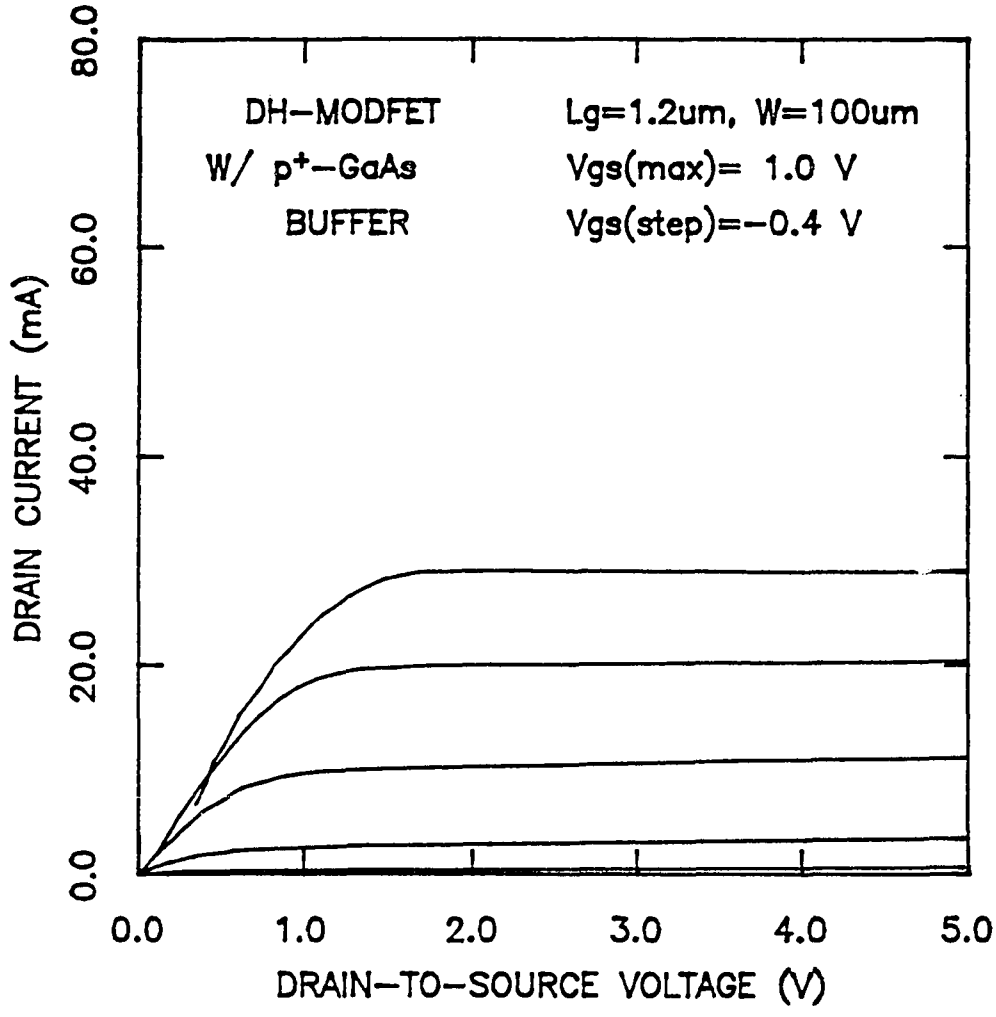

Figure 4.10. I-V characteristics of a 1.2x100 μm DH-MODFET with a buried p^+-GaAs buffer layer.

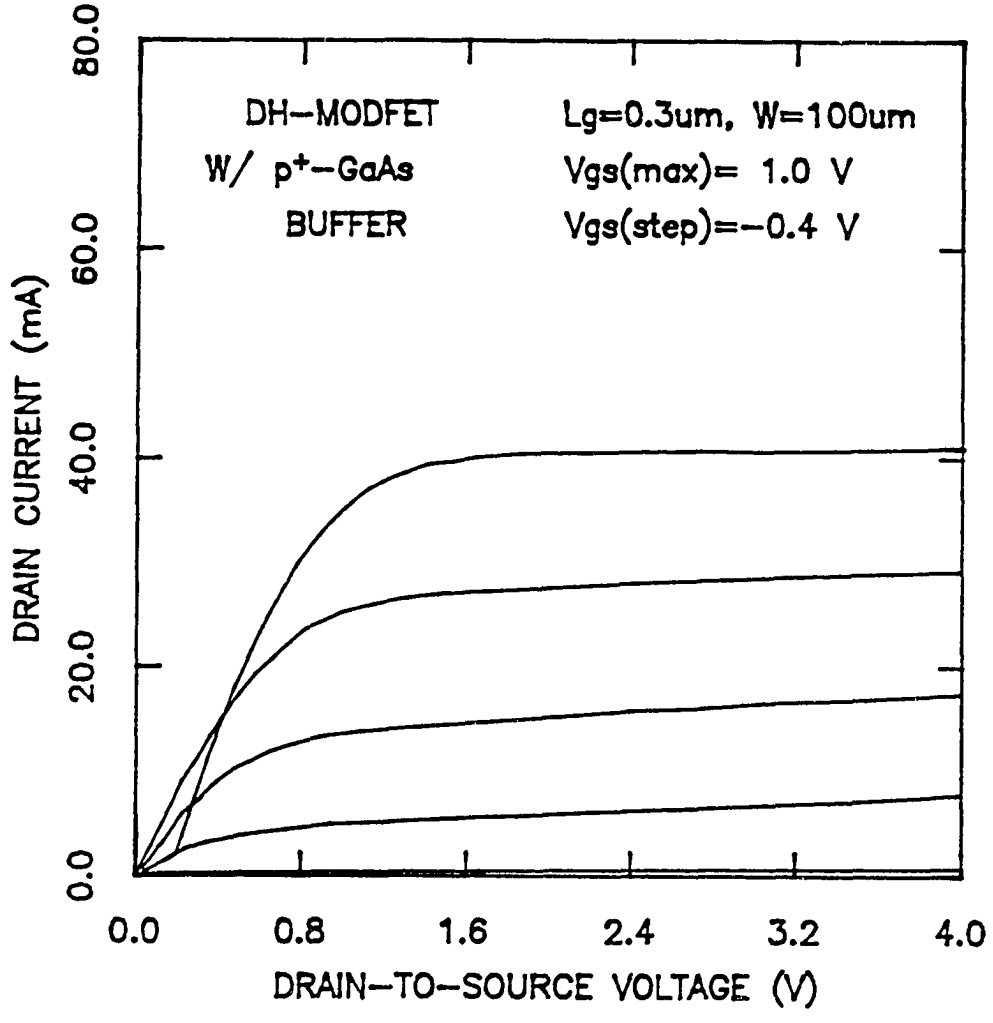

Figure 4.11. I-V characteristics of a 0.3x100 μm DH-MODFET with a buried p^+-GaAs buffer layer.

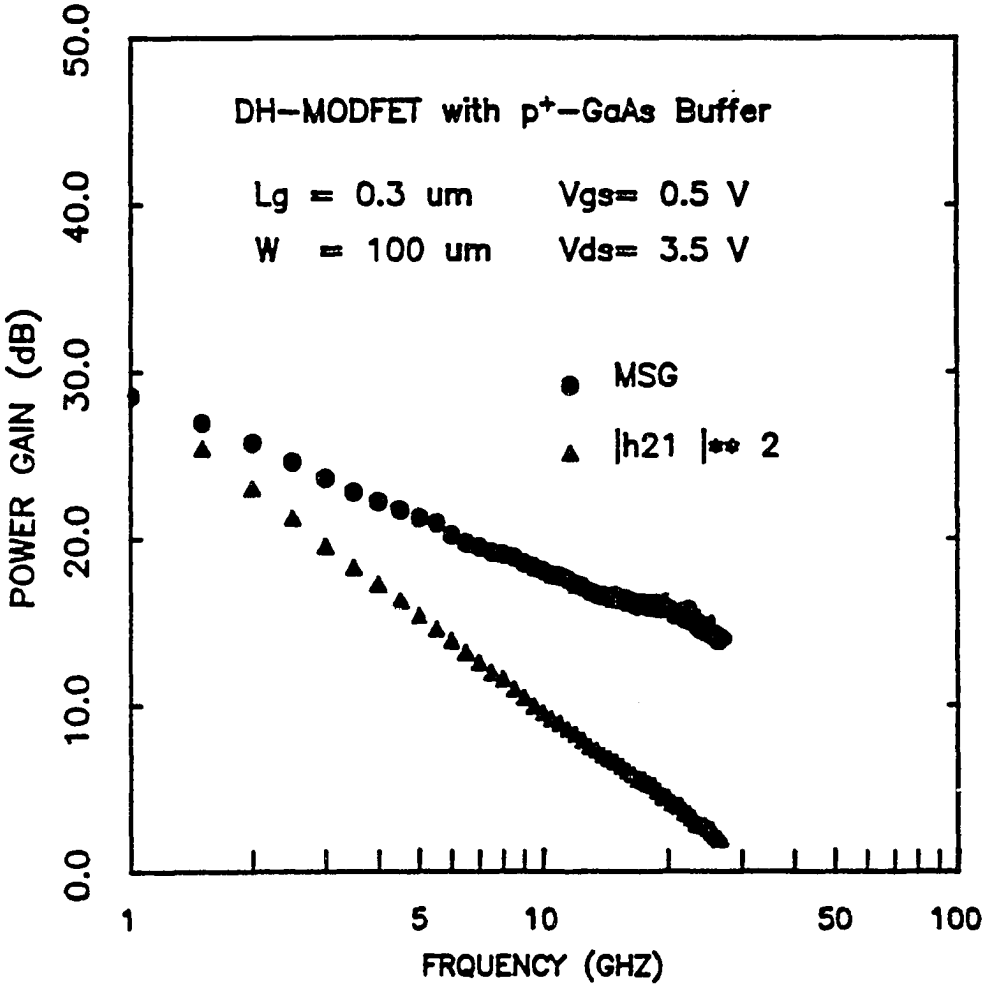

Figure 4.12. Measured power gain versus frequency from a 0.3x100 μm DH-MODFET with a buried p^+-GaAs buffer layer.

density compensated by the p-type acceptors is estimated to be only 5 % from the simulation. However, the f_{MAG} is much better than the DH-MODFETs with superlattice buffer layer due to the improved carrier confinement and the charge control from the higher potential barrier.

DH-MODFETs of 0.3 X 100 μm gate dimension with p^+-GaAs buffer demonstrate the best pinch-off characteristics among those short-channel devices with other buffer configurations, as shown in Fig. 4.11. A full channel current of 480 mA/mm and a g_m of 372 mS/mm are obtained. An f_T of 40 GHz is demonstrated. From measured s-parameter data, the maximum stable gain (MSG) of 14 dB with a stability factor (k) of 0.5 is measured at 26 GHz as shown in Fig. 4.12. This indicates that an f_{MAG} of 180 GHz can be extrapolated. As compared to DH-MODFET with superlattice buffer, this MODFET shows improved gain at high frequency at the cost of lower channel current by using the high barrier p-buffer.

4.5. Summary

In this chapter, the effects of various buffer layer structures on GaAs/InGaAs/AlGaAs DH-MODFETs have been studied. It indicates that high barrier buffers, using superlattice or p-buffer, reduce the carrier deconfinememt and substrate conduction to improve device performance at high frequency. Owing to its higher energy barrier, p-buffer prevents the real space transfer of the hot 2DEG more effectively in the short channel device. On the other hand,

the superlattice buffer improves both the f_T and the channel current with a high quality active 2DEG channel.

It is clear that the merits of both superlattice and p-doped buffer can be combined by using a p-doped superlattice buffer to maintain the quality of active channel and to confine the hot 2DEG electrons.

4.6. References

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CHAPTER 5

HIGH-FIELD INSTABILITY

5.1. Introduction

Since the real-space transfer was first proposed by Hess et al. [1], negative differential resistance (NDR) based on this mechanism had been observed in two-terminal heterojunction structure [2,3] as well as three terminal heterojunction devices such as Negative Resistance Field-Effect Transistor (NERFET) or Charge Injection Transistor (CHINT) [4], HIGFET [5], and GaAs-gate FET [6]. Although the NDR based on real-space transfer is promising to generate high frequency microwave oscillations, so far the success has been limited to 0.025 GHz in a two-terminal device [7], 1.45 GHz from a NERFET [8] and 7.7 GHz from a CHINT device [9]. The low oscillation frequencies are the results of long drifting time of hot electrons in AlGaAs layers in [7] and also the large device parasitics in the case of vertical NERFET or CHINT structures.

The enhanced carrier density as well as reduced output conductance in a double heterojunction Modulation-Doped Field-Effect transistors (DH-MODFETs) are demonstrated in Chapter 4 by utilizing high electron barrier buffer layers such as buried superlattice or buried p^{+}-GaAs layers [10]. With the help from the much reduced carrier injection into the buffer and substrate layers in these

structures, the instabilities generated by the real-space transfer of energetic two-dimensional electron gas (2DEG) into the top wide-bandgap electron supplying layers can then be observed. Negative differential resistance in the DC I-V curves as well as oscillations at microwave frequencies are observed when the Schottky gate is heavily forward biased. This is the first direct observation of the NDR at room temperature in MODFET structures. By studying the relation between the gate current and the drain current in the NDR regime, it is found that the real-space transfer mechanism together with the intervalley k-space transfer in the two-dimensional channel dominates the high field electronic transport properties of the MODFET structures.

The NDR has been observed in the conventional lattice-matched AlGaAs/GaAs/AlGaAs DH-MODFETs as well as in the lattice-strained devices with high barrier buffer layers. All of them utilize the planar-doped (or the δ-doped) AlGaAs layers. The data obtained from the lattice-strained structures, which exhibit larger peak-to-valley ratio and stronger instability at high frequency, will be studied in this chapter. The DC and RF characteristics of the drain NDR will be analyzed in this chapter, and the influence of the real-space transfer mechanism on the gate current and the NDR will also be examined. To demonstrate the microwave generation capability of the NDR in a DH-MODFET structure, an oscillator is built and a fundamental oscillation frequency as high as 19.68 GHz has been obtained. NDR and abnormal gate current are also

LAYER STRUCTURE

400 Å	GaAs:Si (2×10^{18} cm^{-3})
325 Å	undoped $Al_{0.3}Ga_{0.7}As$
	silicon–doped lamina (4×10^{12} cm^{-2})
15 Å	undoped $Al_{0.3}Ga_{0.7}As$ spacer
200 Å	$In_{0.15}Ga_{0.85}As$ Quantum Well
50 Å	undoped GaAs spacer
	silicon–doped lamina (2×10^{12} cm^{-2})
85 Å	undoped GaAs
5,000 Å	superlattice
3,000 Å	GaAs Buffer
GaAs S.I. Substrate (Cut θ=2° off (001), step size= 80 Å)	

Figure 5.1. Layer structure of the DH-MODFET.

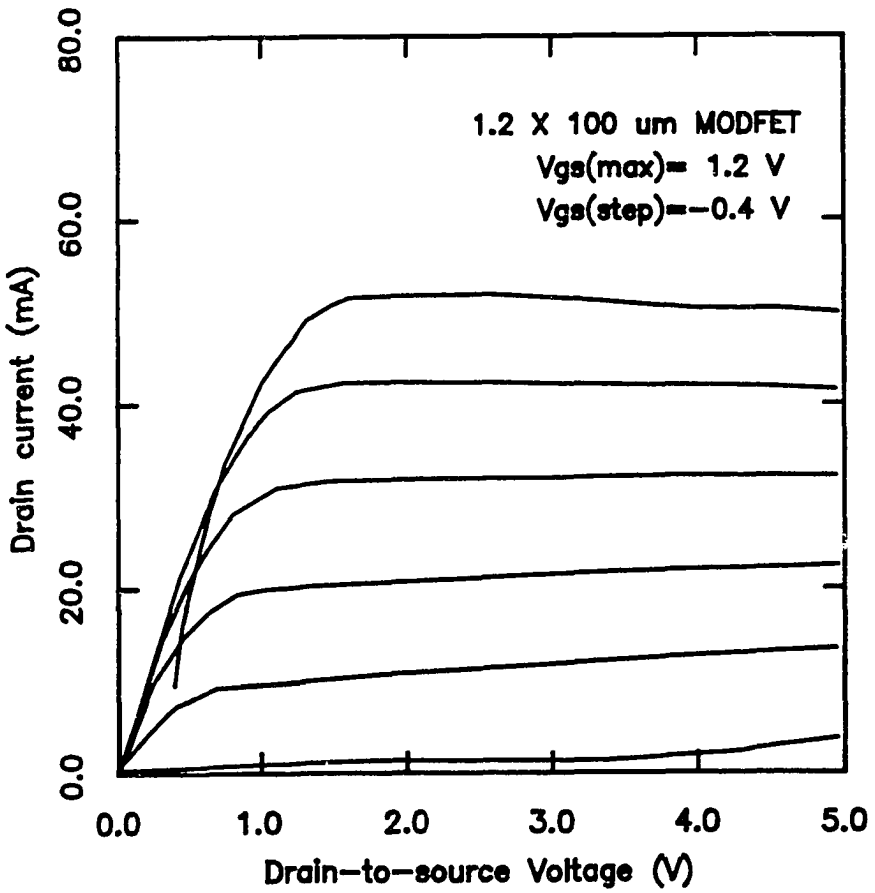

Figure 5.2. DC I-V characteristics of a 1.2X100 μm DH-MODFET.

observed in a multiple quantum-well MODFET structure at room temperature.

5.2. DC and Microwave Characteristics with NDR

5.2.1. DC NDR

The layer structures shown in Fig. 5.1 were grown by MBE on the undoped LEC substrates. The grown wafers are then fabricated with a conventional recess gate 1-um FET process as has been described in Chapter 3. Fig. 5.2 shows the DC drain I-V characteristics of a fabricated DH-MODFET of 1.2 X 100 μm gate dimension. Very good output conductance is obtained at low gate biases, while an NDR can be observed when the gate bias voltage is more than 0.6 volts. The possible NDR resulted from the heating effect of increasing device temperature is eliminated by scanning the Vds from 5 volts to 0 volt at very slow rate.

The gate current (I_g) and the corresponding drain current (I_d) are plotted in Fig. 5.3 where the DH-MODFET exhibits the NDR. At V_{gs}=1.1 V, the gate current (i.e. the lowest dotted curve) is negligible in the FET saturation region. When the gate bias is more than 1.3V, the gate current start turning positive in the FET saturation region. It is interesting to note that the magnitude of the forward gate current corresponds to the magnitude of the NDR. Fig. 5.4 shows the differential current gain ($\beta = -\Delta I_d / \Delta I_g$) curves for a very small amount of perturbation of V_{ds} in the NDR region. The V_{gs} is kept constant when the

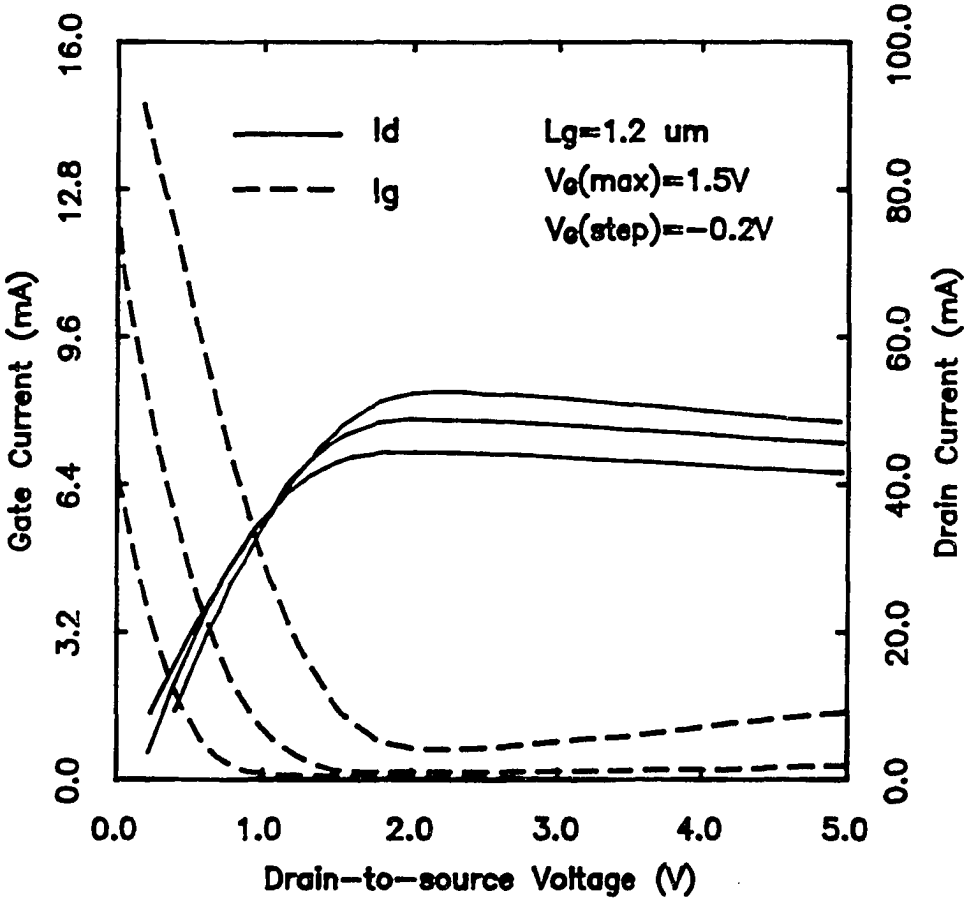

Figure 5.3. Gate and drain current of a 1.2X100 µm DH-MODFET in the NDR region at room temperature.

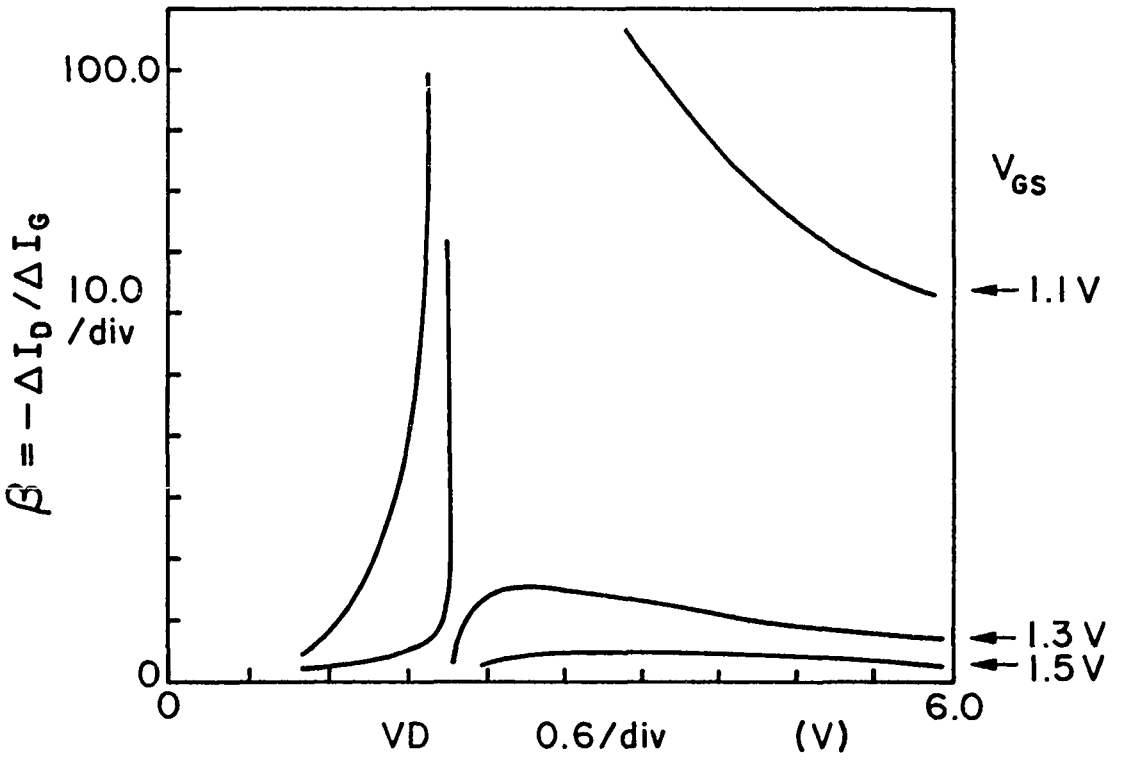

Figure 5.4. Differential current gain (β) of a 1.2X100 μm DH-MODFET in the NDR region at room temperature.

V_{ds} is scanned from 6 V to 0 V. The ratio is very large for a given V_{ds} when the forward gate bias is small, and it decreases exponentially as V_{gs} increases. Eventually the ratio saturated at 2.48 before the large amount of forward Schottky current takes place. This value corresponding to the ratio of the effective saturated electron velocities of the 2DEG channel and the effective electron transit velocity through AlGaAs layer. The behavior of the $-\Delta I_d/\Delta I_g$ can be explained by the real-space transfer of energetic 2DEG into the AlGaAs layer and subsequently removed by the forward-biased gate electrode as part of I_g. The mechanisms of the real-space transfer are the combination of thermionic emission [11], tunneling [12], and k-space assisted tunneling [13] over the barrier from the undoped top AlGaAs spacer layer as will be discussed in the following sections.

5.2.2. Microwave Characteristics of NDR

This DH-MODFET is further probed at microwave frequencies from 0.5 to 26.5 GHz with a pair of Cascade Microtech's wafer probes and an HP 8510 automatic network analyzer. Measured S22 traces at various forward gate biases are plotted in Fig. 5.5 as function of measuring frequency with a constant Vds of 5V. The S22 of a two-port MODFET, with the gate as port #1 and the drain as port #2, is defined as the ratio between the reflected power and the incident power at the drain electrode with the drain as the input port and the gate terminated at a 50-Ω load. When the S22 is greater than unity, the MOD-

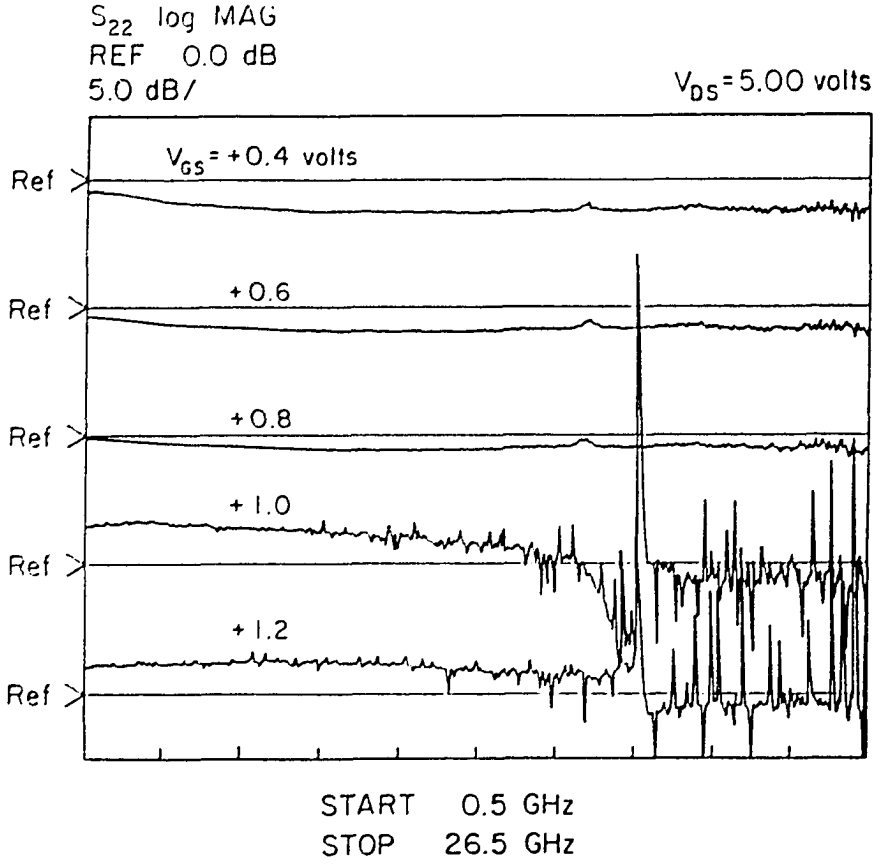

Figure 5.5. S_{22} versus frequency at various V_{GS} with V_{DS}=5 V.

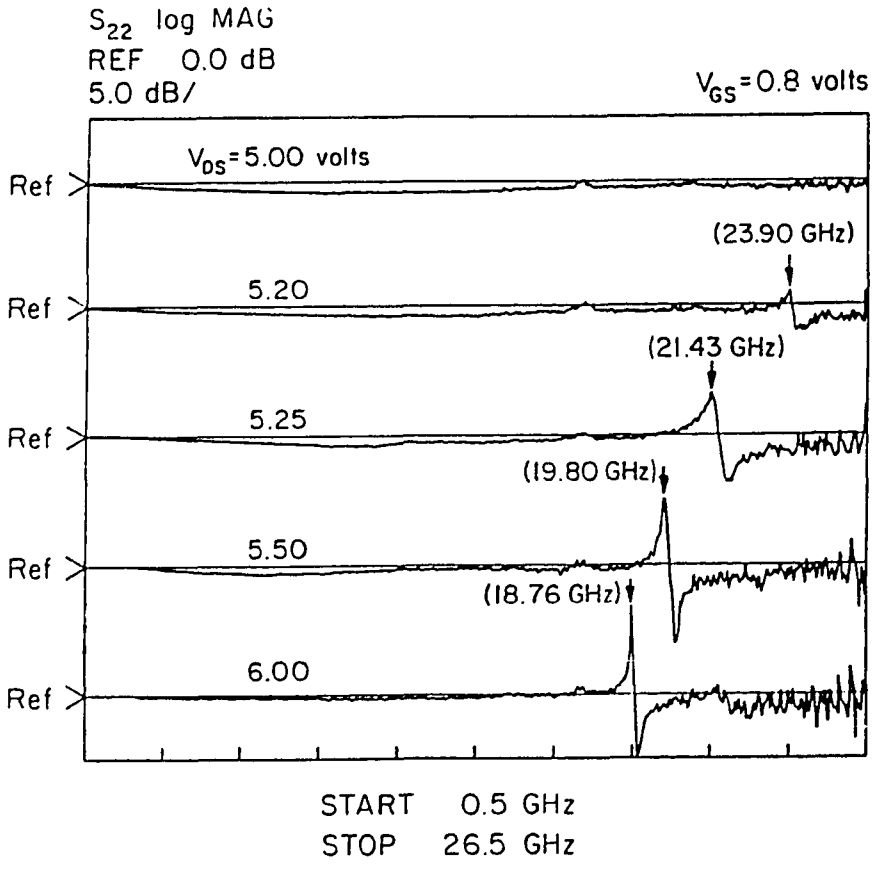

Figure 5.6. S_{22} versus frequency at various V_{DS} with V_{GS}=+0.8 V.

FET sends back amplified RF signal delivered to the drain. In other words, there is a drain NDR when S22 is greater than one. From Fig. 5.5, NDR starts to build up at low frequencies when V_{gs} is more than 0.9 volts. This MODFET eventually bursts into oscillations at 18.7 GHz when V_{gs} is biased more than 1.0 volts. The NDR is only a necessary condition for the device to oscillate. To generate oscillation at a given frequency, the magnitude of negative drain conductance of a MODFET should be greater than all the circuit loss (i.e. positive conductance) presented at the drain terminal. The resonant frequency is determined by all of the device and external circuit parasitics presented at the drain electrode.

The bias-dependent resonant frequencies on various V_{ds} are depicted in Fig. 5.6 with a fixed V_{gs} of +0.3 volts. The resonant frequency of NDR increases from 18 GHz to 24 GHz with the decreasing drain bias potential. This broad variation in the resonant frequency shows there are no traveling domains. This is in contrast to the moving domains which are commonly seen in the Gunn diodes and some GaAs MESFETs with long drift regions [14]. The relatively constant transit time of a moving domain is determined by the velocity of the domain and the geometry of the high field region which change little with the applied drain biases. In our case, the resonant frequency is critically determined by the bias-dependent FET device parasitics, such as the gate-to-source capacitance and gate-to-drain capacitance, and the bias-independent external

circuit parasitics. Because the transconductance of the MODFET is very small under a forward-biased Schottky gate, the oscillation is not generated by the MODFET which serves as a high gain three terminal circuit element. This is further verified by bonding the device in a tuned oscillator circuit where its gate is biased at +1.3 volts and RF-terminated by a 50-Ω impedance, as will be discussed in details in the following sections.

5.3. Possible Mechanisms

The instability can be explained qualitatively by the real-space transfer mechanism of hot 2DEG under a high drain field. As the two-dimensional electrons drifting along the quantum-well channel from source toward drain, some of them acquire enough energy to be real-space transferred into the top or bottom electron supply layers through the undoped spacer layers. As shown in Fig. 5.7, the transfer of the hot 2DEG into the top supplying layer can be achieved by

(1) thermionic emission over the spacer [11],

(2) tunneling through the spacer [12],

(3) first k-space scattered to high valleys of the channel then tunneling over the spacer (i.e. K-space assisted real-space transfer) [13], and

(4) first scattered into the bottom supplying layer or buffer layer then resonant tunneling back into the top supplying layer.

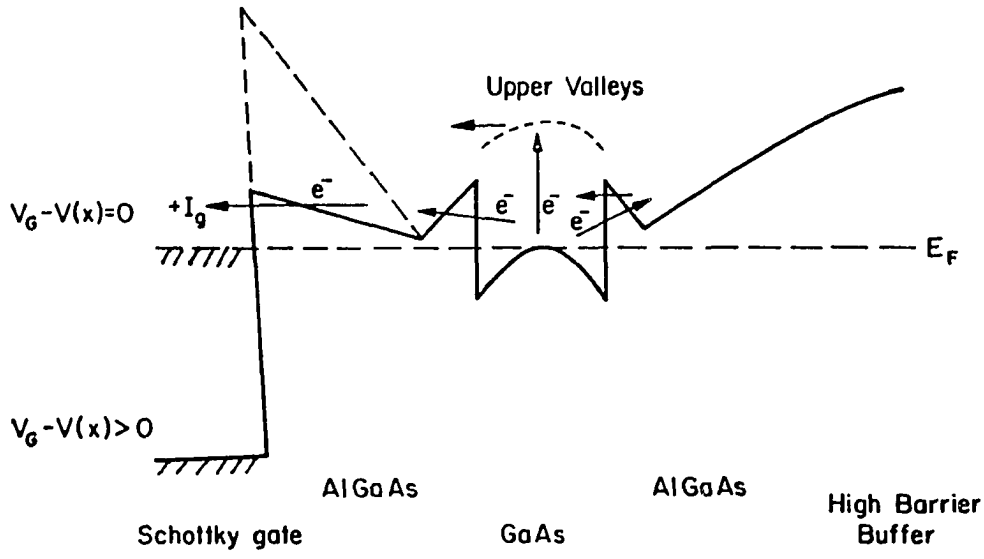

Figure 5.7. Schematic conduction band diagram indicates possible mechanisms for the real-space transfer of hot 2DEG.

When the Schottky gate is reverse-biased, the real-space transferred hot two-dimensional electrons will still contribute a part of drain current by slowly drifting along the quantum-well in the top AlGaAs layer confined by the high Schottky barrier and the undoped spacer layer before they are either neutralized by ionized silicon donors or scattered back to the 2DEG channel. These slow parallel conducting hot electrons in the AlGaAs will decrease the overall drain current density in the short channel devices. In the long channel devices, these real-space transferred electrons will compensate the ionized positive donor ions and lower the effect 2DEG density in the channel which will degrade the FET transconductance and channel current density.

5.3.1. Planar-doped MODFETs

When the gate is forward-biased, the effective Schottky barrier is lowered. This enables some of high energy real-space transferred hot 2DEG in the top AlGaAs layer to reach the the gate electrode as part of forward gate current pre-dominately by thermionic emission over the Schottky barrier. This explains that the exponential dependence of the ratio (i.e. $-\Delta I_d / \Delta I_g$) on the forward V_{gs}.

Eventually, the Schottky barrier will become flat-band under a sufficiently large positive gate potential. Under this situation, only the undoped AlGaAs spacer layer presents a energy barrier between the 2DEG and the positive gate electrode. Once the two-dimensional electrons acquire enough energy (e.g. $\approx \Delta E_C - E_0$ for the thermionic emission) to be real-space transferred into the

AlGaAs layer, they will all be collected efficiently and quickly by the forward-biased gate electrode as part of forward gate current. This explains why the value of the differential drain-to-gate current ratio eventually saturated at large positive gate biases. This also explains why both the NDR and oscillations can only be observed with a relatively high positive gate bias.

5.3.1.1. Differential Current Gain

For a small drain voltage increase (ΔV_d) at a fixed positive gate bias, the differential current gain of the MODFET in the NDR region can be approximated as

$$\beta = -\left[\frac{\Delta I_d}{\Delta I_g}\right]_{V_d}^{V_d+\Delta V_d} \tag{5.1}$$

$$= \frac{\textit{loss of } I_d \textit{ through real-space transferred 2DEG}}{\textit{gain of } I_g \textit{ by real-space transferred 2DEG}}$$

$$= \frac{-\int_{V_d}^{V_d+\Delta V_d} q\frac{dA(V)}{dV}\Delta n_{AlGaAs}(V)\ \langle v\rangle_{2DEG}\ dV}{\int_{V_d}^{V_d+\Delta V_d} q\frac{dA(V)}{dV}\Delta n_{2DEG}(V)\ \langle v\rangle_{AlGaAs}\ dV},$$

where

q is the unity electronic charge,

$\Delta n_{AlGaAs}(V)$ is the amount of real-space transferred 2DEG through a heterointerface area of $dA(V)$ into the top AlGaAs layer,

$\Delta n_{2DEG}(V)$ is the amount of total real-space transferred electrons out of 2DEG through an area of $dA(V)$,

$\langle v \rangle_{2DEG}$ is the average saturated 2DEG drift velocity in the channel, and

$\langle v \rangle_{AlGaAs}$ is the average hot electron drift velocity between heterojunction and the positive-biased Schottky gate.

Here, the gate current model using the average electron drift velocity in the AlGaAs layer is over simplified in the denominator of Eq. 5.1. For the hot electrons in the two-dimensional channel to participate the gate current, they have to overcome two potential barriers; first the potential spike at the heterointerface and then the metal/AlGaAs Schottky barrier. At a high drain voltage, the I_g component from real-space transferred AlGaAs electrons initially increases with V_{gs} from pinch-off to forward biases, and then it saturated at a constant value. The initial increase can be modeled by theories of thermionic emission, field emission, and tunneling of a Schottky barrier. This explains the exponential, Schottky-diode type of dependence on V_{gs} for hot electron gate current and β in Fig. 5.4. After a flat-band situation is established between the metal and undoped AlGaAs layer at high positive V_{gs}, the gate current is only controlled by the potential spike of the spacer layer and β will be saturated.

5.3.1.2. Saturated Differential Current Gain

When V_{gs} is high enough to eliminate the Schottky barrier for the

transferred hot 2DEG, the saturated β value is of some physical importance. If all the real-space transferred 2DEG are transferred into the top AlGaAs electron supplying layer and subsequently absorbed by the positive-biased gate, then $\Delta n_{AlGaAs}(V)$ equals $\Delta n_{2DEG}(V)$. Therefore, Eq. 5.1 can be simplified to

$$\beta = \frac{\langle v \rangle_{2DEG}}{\langle v \rangle_{AlGaAs}} \approx \frac{1.5x10^7\ cm/s}{0.6x10^7\ cm/s} = 2.5\ . \tag{5.2}$$

if a $\langle v \rangle_{2DEG}=1.5x10^7 cm/s$ and a $\langle v \rangle_{AlGaAs}=0.6x10^7 cm/s$ are assumed. This value is very close to the saturated ratio of 2.29 in the experimental data of Fig. 5.4, where the forward Schottky gate current into the parasitic AlGaAs layer and the injected substrate hot electron current may not be negligible.

5.3.2. Uniform-doped MODFET

For conventional MODFET structures with uniformly-doped AlGaAs top supplying layers, a parasitic conduction channel is usually induced in the AlGaAs layer at relatively low gate bias[15]. Without the flat-band condition in the uniformly doped AlGaAs layer, only a small portion of the real-space transferred hot 2DEG may have enough energy to overcome the Schottky barrier and to be collected by the positively biased gate. In this case, the transferred 2DEG may drift along the parasitic AlGaAs MESFET channel or be scattered back to the 2DEG as proposed in [1]. Because the transferred hot carriers may still contribute to the drain current, the NDR effect will not be as

significant as if they are removed completely from the drain current. This small amount of negative differential conductance may easily be shadowed by the large output conductance and was not observed by most of the workers employing uniformly-doped MODFET structures in the past.

5.4. Microwave Generation by NDR at K-Band

To demonstrate the microwave generation capability of the NDR in the DH-MODFET, an oscillator was assembled with a 1.2-μm gate MODFET. The device was first wired-bonded in a micro-strip chip carrier and then inserted into a microwave test fixture. Fig. 5.8 shows the circuit diagram of the oscillator where two bias-tee's are used to supply the necessary gate and drain current. A spectrum analyzer (HP8569A) with 50-Ω input impedance is utilized to monitor the possible oscillation.

The gate is RF-terminated with a broadband 50-Ω resistor to guarantee a resistive termination at the gate electrode and to minimize any possible reactance generated by the connection 50-Ω cables. As discussed in the previous sections, the NDR alone is not enough to generate oscillation. The oscillation can only be initiated when the magnitude of the NDR is less than all the load resistance presented at the drain. Because of the small peak-to-valley ratio of the drain NDR, which is in the order of 1.3 kΩ for the 1.2 X 100 μm MODFET, a double-slot tuner is utilized to transform the 50-Ω load impedance of the input of the spectrum analyzer to a high resistance value presented at the drain

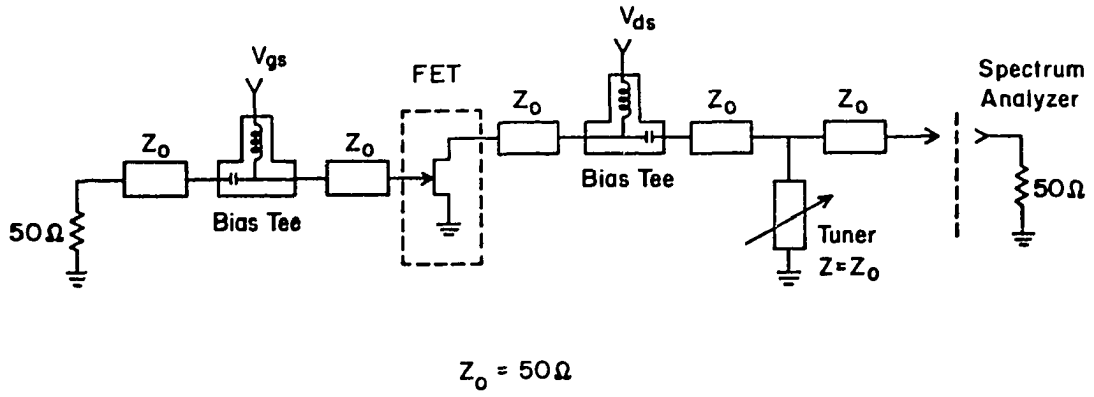

Figure 5.8. Circuit diagram of a microwave oscillator utilizing the drain NDR.

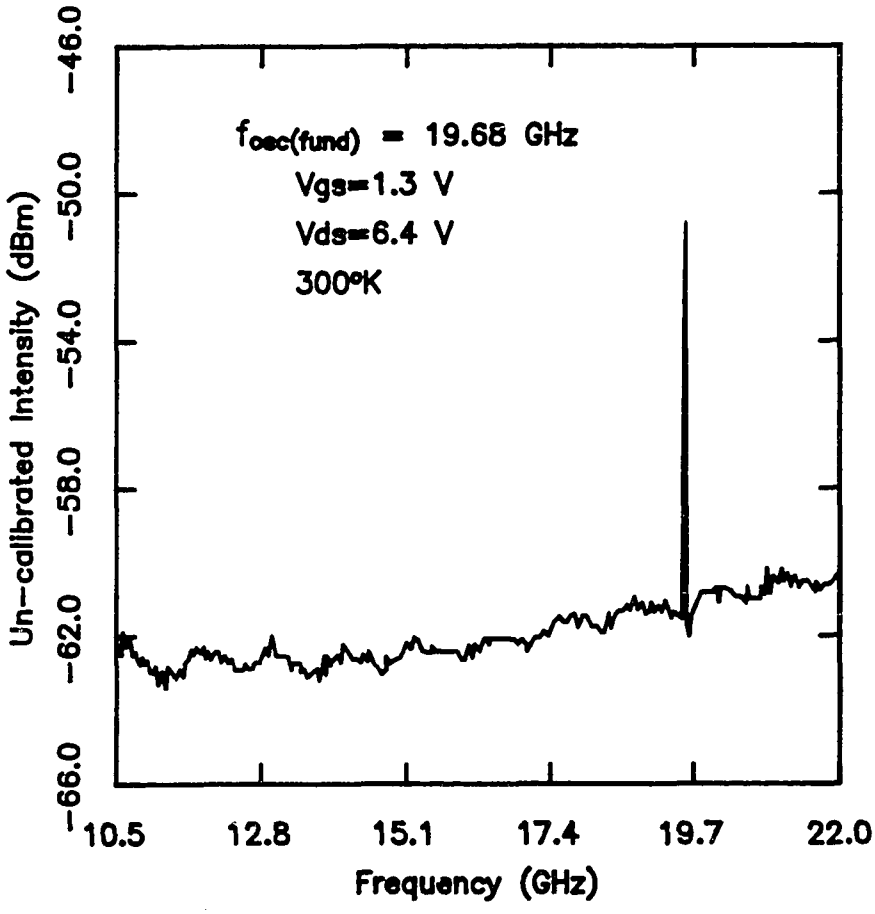

Figure 5.9. Spectrum analyzer trace indicating a fundamental oscillation frequency of 19.68 GHz at room temperature.

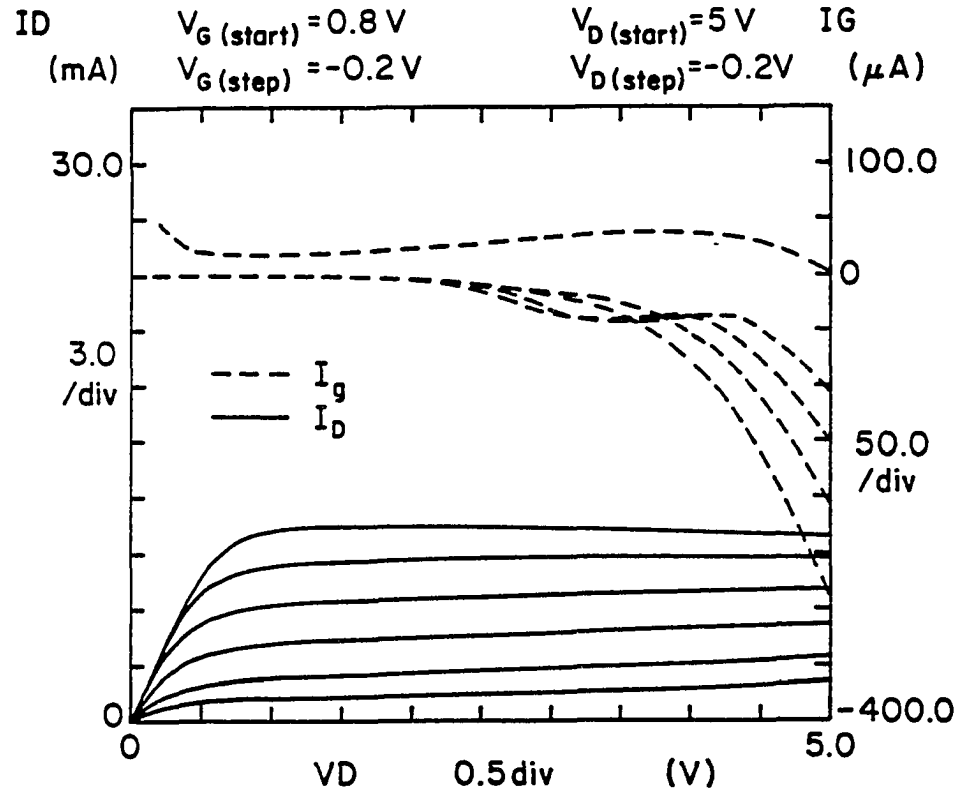

Figure 5.10. I_D and I_G of a double quantum-well MODFET with 0.3-μm gate length operated in the NDR region.

terminal. Once the net resistance at the drain terminal is negative, the drain circuit will oscillate at the resonant frequency which is determined by both the internal device parasitics and the external circuit parasitics. A fundamental oscillation frequency as high as 19.68 GHz can be generated at the drain circuit as shown in Fig. 5.9 recorded by the spectrum analyzer. However, the efficiency of generating the fundamental frequency is low due to the small peak-to-valley ratio of the drain current in the NDR region. The efficiency can be improved by increasing the peak-to-valley ratio with a lower heterojunction barrier to facilitate the transfer of the energetic 2DEG and a normally-off MODFET structure to reduce the quiescent drain current.

5.5. NDR in a Multiple Quantum-Well MODFET

The fabrication and characterization of a high-current planar-doped AlGaAs/InGaAs pseudomorphic double quantum-well MODFETs was reported in [16]. At 300 K the 0.3-μm gate devices show a full channel current of 1100 mA/mm with a constant extrinsic transconductance of 350 mS/mm over a broad voltage range of 1.6 volts. f_{MAG} of 110 GHz and f_T of 52 GHz have been demonstrated from small signal s-parameter measurements. An NDR is also observed in the I-V characteristics of this device at high forward gate biases. Only the the NDR of this device will be review in this section, while the related device characteristics can be found in [16].

The gate current and the corresponding drain current in the NDR region are depicted in Fig. 5.10. At V_{gs}=0.8 volts, there is a forward gate current which results in the decreasing of the corresponding drain current. This is quite similar to the double heterojunction MODFET as discussed in the previous section. Because of the low gate-to-drain breakdown voltage of this device, the magnitude of the reverse breakdown current could be larger than the forward gate current generated by the real-space transferred hot 2DEG. The reverse breakdown gate current also exhibits a few peaks at V_{gs}= 0.4 and 0.6 volts. These peaks in I_g are probably the results of the resonant-tunneling of breakdown current through the multiple quantum-wells.

5.6. Summary

The real-space transfer of the energetic 2DEG into the supplying layers should exist for either single or multiple heterojunction structures at any gate bias conditions under a sufficient high accelerating field as proposed in [1]. However, it is more pronounced in our MODFET structure where less amount of 2DEG is lost to the substrate current, and the planar doped top AlGaAs layer provides a flat-band condition to physically remove the real-space transferred hot 2DEG from the drain current and become part of forward gate current.

The transit time for the hot electrons to travel through the very thin top undoped AlGaAs supplying layer between the 2DEG and the forward-biased gate could be very short. This short transit time, together with the very small

external device parasitics in a lateral MODFET structure, result in the NDR suitable for the high frequency generation. Microwave generations up to 24 GHz have been demonstrated by a DH-MODFET of 1.2-um gate length under forward biases. However, the efficiency of generating the fundamental frequency is low due to the small peak-to-valley ratio of the drain current in the NDR region. The efficiency can be further improved by increasing the peak-to-valley ratio with a reduced spacer barrier and a normally-off MODFET structure. Nevertheless, this observation proves the real-space transfer is one of the most important and dominating device dynamics in the MODFET structure. The short transit time of the NDR demonstrated in this case is very promising for the microwave and millimeter-wave generations.

The carrier deconfinement of the hot two-dimensional electrons by the real space transfer mechanism would present a limiting factor for MODFET applications. Enhanced device performance would be resulted, such as a larger current density, higher output conductance, and reduced buffer current, if high potential barriers are incorporated in designing the spacer and buffer layers.

5.7. References

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CHAPTER 6

PICOSECOND MODPCDS

6.1. Introduction

In recent years, the optical communication system has attracted a lot of interests as a fast, reliable, and secure tool for both short haul and long distance information exchange. Because most of the semiconductor light sources, such as lasers and LED's, are fabricated on the compound semiconductors, it is very desirable to integrate the whole optical transceiver on the same chip using the OEIC (Opto-Electronic Integrated Circuit) technology. Various optical detectors for the easily monolithic integration with the commercially available GaAs MESFET technology have been studied [1,2].

However, the maximum operating speed provided by the state-of-the-art GaAs MESFET technology is limited to 20GHz [3] or a single-stage propagation delay of 10ps [4]. On the other hand, with almost identical fabrication technology as GaAs MESFET's, Modulation-Doped Field-Effect Transistors (MODFET's) or High Electron Mobility Transistors (HEMT's) have demonstrated very high cut-off frequencies [5], low-noise amplification [6], and sub-10ps propagation delays [7,8]. A risetime of 12 ps and a full-width at half-maximum (FWHM) impulse response of 27 ps were obtained from a three-terminal MOD-

FET with a gatelength of 20-μm with a very high external quantum efficiency of 6.3 [9]. Umeda et al. has measured an impulse response of 22 ps (FWHM) from a HEMT structure with 2-μm gatelength [10]. Both reported data in [9] and [10] have been corrected for the the external parasitics and the finited pulsewidth of the optical source with a correlation technique from a pair of detectors. A monolithic integrated receiver front end of a photoconductive detector and a selectively doped heterostructure transistor was also demonstrated with a measured gain-bandwidth product of 5 GHz and a 3dB bandwidth of 500 MHz limited by the traps in the epitaxial layers [11].

In this chapter, the optical response of Modulation-Doped Photoconductor Detectors (MODPCD's) will be studied. MODPCD's are two-terminal devices, which provide more light-sensitive area than MODFET detectors and can be direct integrated with MODFET's on the same wafer. Section 6.2 describes the fabrication process of the MODPCD/MODFET amplifiers and briefly introduces the 800-nm pulse measurement techniques established by Wojtczuk [12]. Various excitation and recombination mechanisms in both the two-dimensional quantum-well and the buffer, which determine the speed and gain of MODPCD's under the illumination of picosecond light pulses, will be reviewed in Section 6.3.

The optical penetration depth of the 800-nm light is approximately one-micron deep into the bulk GaAs material [13], which is more than ten times

deeper than the active epitaxial layer thickness needed for MODFET operations. Therefore, the type and quality of a buffer layer will have different impacts on the performance of MODPCD's and MODFET's in a monolithic photoreceiver. Picosecond optical responses from the MODPCD's and microwave characteristics from their monolithically integrated MODFET's are analyzed from three modulation-doped heterostructures of different material qualities and layer designs. Very fast optical response with a FWHM of 31 ps as well as a sharp risetime of 2 ps have been demonstrated. Very high external optical gain of 1,860% is also demonstrated on a MODPCD with a buried p^+-GaAs buffer layer. The influence of various buffer layer configurations on optical responses of MODPCD's and electrical characteristics of integrated MODFET's will be reported and examined in Section 6.4.

6.2. Fabrication Processes and Measurements

The individual processing step for the MODPCD/MODFET photoreceiver is identical to what is used to fabricate MODFETs in Chapter 3. Detailed descriptions of optical testing arrangements used in this chapter can be located in [12]. The following section provides a brief review of what have been utilized to fabricate and measure these detectors. Because no precision correlation experimental techniques were established on our primitive optical set-ups to determine the intrinsic device response, these reviews on the processing and measurement limitations will be very informative when our results are compared to those pub-

lished intrinsic device data.

6.2.1. Fabrication Process

The sequence of lithographic steps have been modified from the baseline MODFET process listed in Chapter 3 to accommodate two additional steps: (1) selectively deposition of a dielectric isolation layer between the top and the bottom interconnection layers, and (2) recess-etching the epilayers of MODPCD's. To avoid excess mask steps, the bottom interconnection layer utilizes the ohmic metal and the top interconnection layer is the same level as the gate metallization. The isolation between the top and bottom layers is accomplished by inserting an evaporated aluminum oxide dielectric insulating layer with a lift-off process. The following paragraphs briefly describe the sequence of lithographic steps to complete a monolithic optoreceiver.

i) mesa etch

Establish the electrical isolation among active devices by using wet chemical etchants to selectively remove the active epitaxial material between devices.

ii) ohmic metal formation

Forming the source/drain ohmic contacts and bottom level of interconnections with a lift-off process and following by a sintering cycle of 450 C for 5 seconds. The metallization layer used is Ni/AuGe/Ag/Au of 100A/ 1000A/ 1000A/ 2500A.

iii) dielectric isolation layer

Deposit 2000A thick Al_2O_3 insulating layer on the selected area of ohmic metal lines, where top metal lines will cross-over. This step is done by evaporating Al_2O_3 and lift-off.

iv) gate and top interconnection

The pattern of the 1-μm gate and interconnection lines are first defined by a mid-UV contact aligner. The MODFET channel are then proper recessed to the desired current density. Multiple metal layers of Ti/Pd/Au (400A/ 400A/ 3000A) are evaporated and lift-off to form the Schottky gate, top interconnection lines, and bonding pads.

v) recess of MODPCD's

The last lithographic step is done to reveal the active areas of the interdigitated photodetector and to protect other active devices. The dark current of the MODPCD's is then adjusted to the desired value by wet chemical recess.

vi) backside process and packaging

Once the last layer of photo-resist is removed, the complete circuit is waxed face-down on the lapping disc. The substrate of the wafer is thinned to 125-150 microns by mechanical lapping and polishing. A diamond-tipped scriber is used to dice the wafer into individual devices or circuits. The diced MODPCD is then mounted on a high-speed SMA header with silver epoxy. The device is ready for optical and electrical testing after the electrodes are wired to posts of

the SMA header.

6.2.2. Measurement of Impulse Response

The optical source is an 800nm AlGaAs/GaAs laser emitting 32ps FWHM pulses with 1MHz repetition rate. A factory-calibrated AlGaAs/GaAs PIN diode with a known external optical gain (75%) is used as the reference to evaluate the optical gain of other detectors. Detailed descriptions on how to set up an test detector under the same radiation pattern as the reference detector can be found in Section 2.4 of [12]. The micro-photograph of a fabricated MODPCD is shown in Fig. 6.1. A two-stage direct-coupled MOPCD/MODFET photoreceiver fabricated on the same wafer is shown in Fig. 6.2. Because of the limited power supply leads of the test fixture, the receiver was not characterized. The active area of this inter-digitated detector is 40 x 60 $(\mu m)^2$ with a 2-μm finger width and 2-μm finger-to-finger spacing. Because of the absence of anti-reflection coating (about 30% light loss) and the interdigitated layout (about 50% loss of light-sensitive area), these processing related issues limit the external quantum efficiency to only 35% of the internal efficiency.

To remove the effect of finite laser pulse width (31 ps) in the detector response, a simple de-convolution process can be performed. Assuming both shapes of the laser pulse and the detector response are Gaussian, the FWHM of the detector which is proportional to the square root of variance of a Gaussian curve can be de-convolved from the measured response by [1]

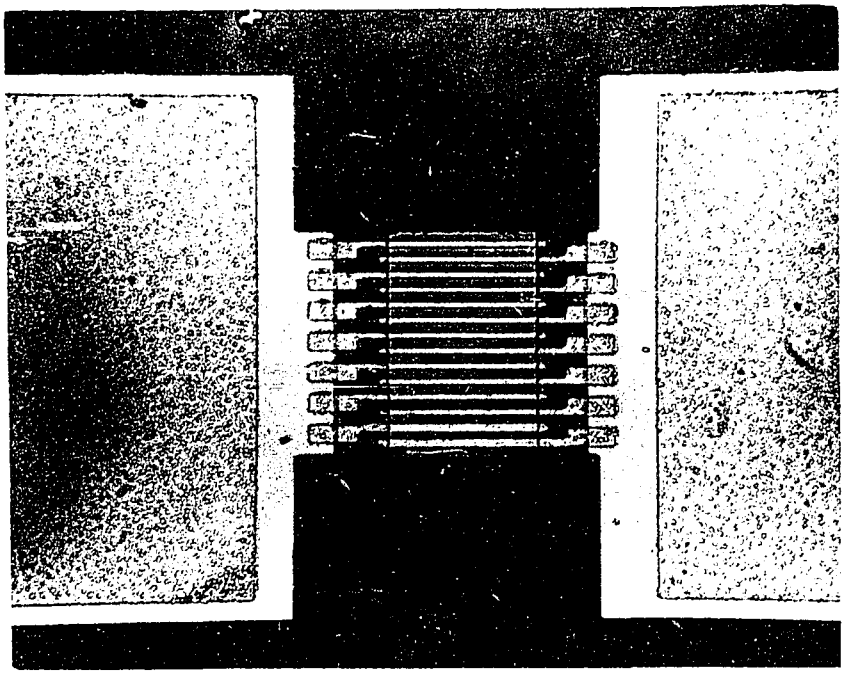

Figure 6.1. A fabricated MODPCD on a 40 X 60 $(\mu m)^2$ mesa with 2-μm finger width and 2-μm finger-to-finger spacing.

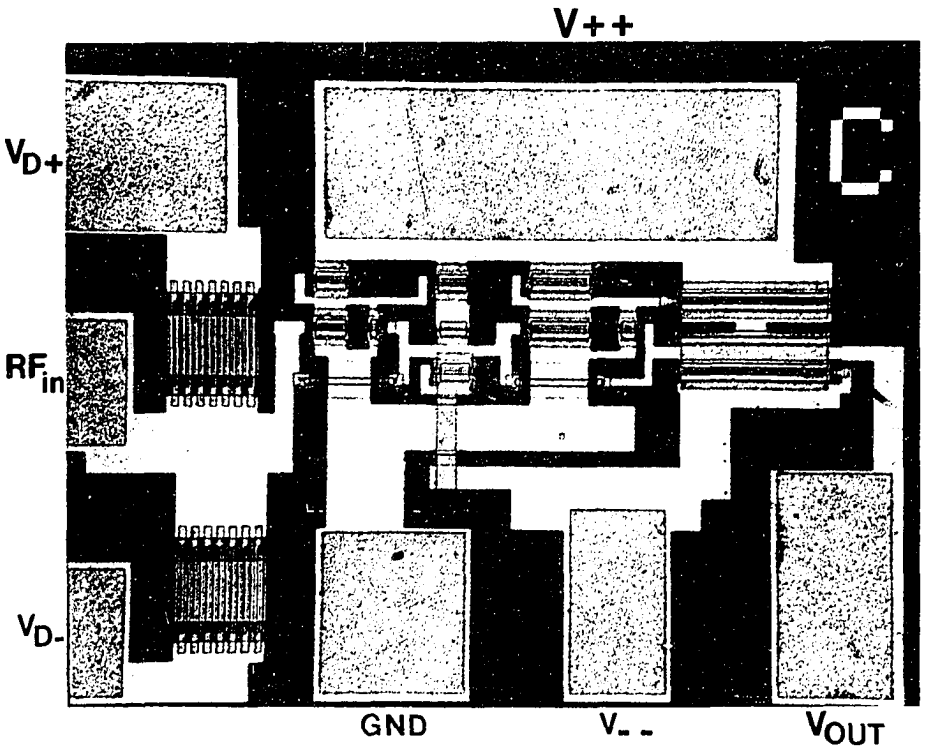

Figure 6.2. A fabricated two-stage direct-coupled MODPCD/MODFET integrated photo-receiver.

$$(FWHM_{detector})^2=(FWHM_{observed})^2-(FWHM_{laser})^2 \quad . \tag{6.1}$$

6.3. Optical Response

Generally, the performance of an optical detector is evaluated in terms of three parameters: the optical gain, the response time, and the noise performance (or the specific detectivity). Only those device parameters of the MODPCD's, which influence the gain and speed, will be examined in this chapter. The most important and interesting figure-of-merit of an optical detector, the detectivity, will be left out for future studies, because our set-ups were not adequate to perform the detailed measurements on its noise behavior.

Since the penetration depth of the 800nm light source is in the order of a micron in GaAs, it is almost ten-times the thickness of the active epitaxial layer thickness needed to fabricate a MODFET in an integrated amplifier. Therefore, the optical response of these integrated MODPCD's will be influenced by both the two-dimensional quantum well and the bulk GaAs buffer/substrate layer. In this section, mechanisms responsible for the gain and speed under picosecond light illuminations will be discussed.

6.3.1. Steady-State Bulk Response

For a bulk semiconductor detector under a uniform above-bandgap illumination, the internal optical gain $G_{internal}$, that is defined as the number of excess carriers flowing into ohmic terminals divided by the number of photons absorbed in the semiconductor, is

$$G_{internal} = \frac{\Delta I}{q I_{ph}} = \frac{\tau_n \mu_n F}{L} + \frac{\tau_p \mu_p F}{L} \tag{6.2}$$

where F is the low electrical field, L is the spacing between two adjacent electrodes, τ_n is the lifetime of excess electrons, τ_p is the lifetime of excess holes, μ_n is the low-field drift mobility of excess electrons, μ_p is the low-field drift mobility of excess holes and I_{ph} is the number of absorbed photons. The external gain is related to the internal gain by

$$G_{external} = \eta G_{internal}, \tag{6.3}$$

where η is the internal quantum efficiency. The internal gain $G_{internal}$ can be rewritten in terms of the electron transit time ($\tau_{rn}=L/v_n$) and the hole transit time ($\tau_{rp}=L/v_p$) as

$$G_{internal} = \frac{\tau_n}{\tau_{rn}} + \frac{\tau_p}{\tau_{rp}}, \tag{6.4}$$

where $v_{n,p}=\mu_{n,p}(F)\,F$ are the average velocities of excess electrons and holes under the electrical field F. This generalized equation is valid and independent of device geometries, carrier dynamics, and recombination processes as long as: 1) there is no avalanche gain, and 2) the lifetime is interpreted as the average time of photo-generated carriers contributing to the excess current [14]. To obtain a fast response time, the inter-electrode spacing L is usually made very small, and the contribution from the electronic transit time (i.e. the first term in Eq. 6.4) dominates the $G_{internal}$ in the GaAs material system. And

$$G_{internal}=\frac{\tau_n}{\tau_m}. \tag{6.5}$$

Obviously the photoconductive gain is greatest when the lifetime is long and when closely spaced contacts are used on a material with high-mobility and high drift velocity.

The steady-state gain-bandwidth product, that is proportional to $G_{internal}/\tau_n$, is then inversely proportional to the electron transit time ($\tau_m=L/v_n$) in GaAs, while a fast response time and broad-band operations require short effective excess carrier lifetime (τ_n). A detector with a high gain-bandwidth product can be realized with closely spaced contacts (L) and high carrier drift velocity (v_n). Because the linewidth of contact fingers is limited by the resolution of lithographic processes, the quantum efficiency and the external gain will be suffered if the light-sensitive area is reduced by the small inter-electrode spacing. The maximum gain-bandwidth product of a photoconductive detector, however, is limited by the inverse of the dielectric relaxation time of the semiconductor [15] which is in the order of a picosecond for a trap-free intrinsic GaAs material.

6.3.2. Picosecond Bulk Response

The internal response time of a photoconductive detector is determined by the absorption/generation processes of excess carriers, the transit time of the excess carriers, and the effective lifetime of the excess carriers. The intrinsic risetime of the photocurrent is determined by the dynamics of absorbing a photon and subsequent generation of an excess electron-hole pair. Once excess

carriers are generated, they are governed by drift-diffusion equations of charge carriers, the charge neutrality, and various recombination and generation mechanisms [16,17]. The observed external risetime and falltime of the detector in response to a incident light pulse will also be determined by the shape of the incoming laser pulse, the internal device parasitics (such as the interelectrode capacitance and the output conductance of the detector), and the external circuit elements connected to it.

6.3.2.1. Transit-Time Limited Response

The effective electron lifetime τ_n is determined by the lifetime of the excess photo-generated electron-hole pairs. If the interelectrode spacing L is very small and the saturated electron drift velocity (v_n) is much larger than the hole drift velocity (v_p), the primary photo-generated electrons will reach the electrode earlier than the primary photo-generated holes. Extra secondary electrons have to be injected from the electrode to maintain the charge neutrality in the semiconductor. Under this circumstance, τ_n, which is defined as the effective electron lifetime contributing to the photocurrent, equals the average photo-generated hole transit time (τ_{rp}). That is,

$$\tau_n = <\tau_{rp}> = \frac{L}{v_p}; \tag{6.6}$$

and the transit-time limited internal optical gain is

$$G_{internal}=\frac{<\tau_n>}{<\tau_{rn}>}=\frac{<\tau_{rp}>}{<\tau_{rn}>}=\frac{<v_n>}{<v_p>}. \quad (6.7)$$

Once photo-excited primary carriers are captured by traps or other slow recombination mechanisms, the slowly released primary minority carriers will induce the more injected secondary carriers with an opposite charge parity from electrodes to maintain the charge neutrality and increase the effective carrier lifetime. This long free-carrier lifetime will increase the optical gain at the expense of attaching a long-lasting tail to the pulse response. The long tail greatly reduces the 3dB bandwidth of the detector and makes a low-pass equalizer necessary for real applications where flat frequency responses are needed [9].

In the photoconductive detector, a strong lateral electrical field is usually presented across the active channel by the external bias to accelerate excess carriers and to improve the output conductance of the detector. Because most of the light sensitive channel in the transit-time limited photoconductive detector is under the high field, its optical gain can be adequately expressed by [18,19]

$$G_{internal}=\frac{\tau_p}{\tau_{rp}}(1+\frac{\mu_n}{\mu_p})[1-e^{-L/\tau_p v_p}]. \quad (6.8)$$

6.3.2.2. Femtosecond Photo-Excited Carrier Dynamics

The dynamics of photo-excited carriers in GaAs are very important for both understanding the physics of semiconductor and determining the fundamental speed limitation of the electronic circuits, and currently are still under very active investigation. These time constants together with the picosecond transit-time of

excess carriers near the electrodes limit the intrinsic device risetime response under an ideal impulse-type light illumination. These time-constants are governed by the uncertainty principle, conservation rules and selection rules from various scattering dynamics [20,21].

When an optical impulse interacts with the semiconductor, it first generates electron and hole pairs through interband absorption. This quantum mechanical process is very fast, and its time-constant can be approximated by the uncertainty principle (i.e. in the order of 0.3 fs for a bandgap of 1.4 eV in GaAs). The initial energy distribution of these excited carriers is determined by the energy and spectrum of the incident optical pulse. High energy carriers are first relaxed from the initial photo-excited non-equilibrium distribution to a quasi-equilibrium state at a carrier temperature much higher than the lattice temperature through carrier-carrier and carrier-phonon scattering. This relaxation to the quasi-equilibrium is very fast with a time constant in the order of 10 to 35 fs which is obtained by experimental femtosecond probing techniques by Tang [22-25]. This first stage relaxation time depends on the carrier density as well as energy distribution, and scattering of energetic carriers into high valleys is also observed [25] and derived theoretically [24].

This quasi-equilibrium hot carrier distribution will then cool down to the lattice temperature. In GaAs it is known that the excited electrons and holes will relax toward their respective band extrema through a cascade of *LO*-phonon

emissions. The time to emit a *LO* phonon has been estimated to be ~0.1 ps. The picosecond room-temperature relaxation time for this carrier-cooling and state-filling at bandedge has been experimentally studied with a picosecond optical probing technique by Shank et al. [26], and is in the order of 1.7 to 1.3 ps for GaAs with a carrier density range of 0.5 - 2.0 x 10^{19} cm^{-3} [27]. Therefore, the room-temperature time delay to complete the relaxation process (from the absorption of a photon to a pair of cool electron and hole) is in the order of 1-2 ps. This response time will also be influenced by the operating electrical field, the lattice temperature, and the dark current of charged carriers. However, from these published data, it is fair to say that the room-temperature intrinsic detector response time is about 1 to 2 ps under the illumination of an impulse-like light pulse. The external pulse response of detector $I(t)$ is the time convolution of the waveform of light source $S(t)$, impulse response of intrinsic detector $G(t)$, and the impulse response of device and external circuit parasitics $H(t)$ as

$$I(t) = S(t) * G(t) * H(t). \tag{6.9}$$

In the absence of the external circuit elements H(t), the intrinsic detector response can be expressed as

$$I(t)=\int_0^{\infty}\int_0^{L} G(x-v_n t)\, S(\tau-t)\, dx\, d\tau \tag{6.10}$$

or,

$$=\int_0^{\tau_n}\int_0^{L} G(x-v_n t)\, S(\tau-t)\, dx\, d\tau$$

where τ_n is limited by either the lifetime or the transit time of of excess minority carriers. The risetime of the intrinsic detector can be obtained in the similar manner, but its minimum is limited to about 1 ps by the absorption/generation process.

For an interdigitated GaAs MODPCD with a 2-μm gap, the electron transit time (τ_m) will be about 20 ps with a saturated electron velocity of $1x10^7$ *cm/s*. If the duration of the laser pulse is only a few picoseconds, the equilibrium between the fast optical excitation processes of excess carriers and the usually slow annihilation processes in the semiconductor may not be established before the light is turned off. Therefore, even the onset of the photoconduction by a picosecond light pulse is very fast, the internal detector response time is dominated by the decay time constants of the excess charge carriers. The internal gain will then be reduced to [28]

$$G_{internal} = \frac{\Delta t_p}{\tau_m}, \qquad \text{for } 0<t<\Delta t_p, \tag{6.11}$$

$$= \frac{\Delta t_p}{\tau_m} e^{-t/\tau_n}, \qquad \text{for } \Delta t_p<t,$$

where Δt_p is the duration of the laser pulse, τ_m is the electron transit time between two adjacent electrodes, and τ_n is the effective lifetime of excess electrons. The falltime of the internal photo-response is determined by various recombination processes and the number of excess electrons and holes actually participating these processes. Various picosecond optical responses of

MODPCD's under different trapping mechanisms, such as buffer defects and hole-traps in a buried p^+-GaAs buffer, will be studied in the following sections.

6.3.3. Photo-Response of Two-Dimensional System

Interest of light scattering by two-dimensional systems in semiconductors was first stimulated by Burstein et al. [29]. Recent developments in this field can be found in a few good review papers [30-32]. Multiple Quantum Well (MQW) devices which have unique properties, such as free excitons in quantum wells [33] and the quantum-confined Stark effect [34], have generated a new technology for opto-electronics. New devices such as optical modulators [35], new avalanche superlattice detectors[36], FET-like optical gated modulators and charge storage devices [37], etc. Some mechanisms which affect the performance of MODPCD's will be reviewed briefly in this section.

Burstein pointed out that within the effective mass approximation, the mechanisms and selection rules for light scattering by a two-dimensional (2D) semiconductor plasma are similar to those of the three-dimensional (3D) systems. After the absorption of a femtosecond light pulse in the quantum well, there will be two-step relaxation/cooling process similar to the 3D process. However, the photoexcited hot electron-hole carriers will be subjected to different carrier-carrier and carrier-phonon interactions with different distribution functions, subbands, and the real-space transfer mechanism. The initial intraband carrier relaxation time of hot carriers is in the order of 35 fs at room

temperature which is faster than the 3D case, and will be shorter with high carrier density [38]. The decay time-constant for the following cooling or band-filling process is in the order of 1 ps [39] for absorptions inside the quantum well and 7 ps [40] for a photon energy greater than the energy gap of the barrier layer (AlGaAs), and it is longer than what is typically measured from a bulk sample.

At room temperature, excitons could be generated in undoped MQW's under low light intensity [33]. However, they can be bleached-out to become free electron-hole carriers very quickly by the ionization process with optical phonons in the presence of an in-plane electric field [41] or a large amount of two-dimensional free electrons in quantum wells (which are needed for MODFET's). The total absorption process occurs within 500 fs [42]. A minimum intrinsic response time for a lateral MODPCD, which is operated with an in-plane electrical field and non-zero dark current, can be estimated to be in the order of 1 ps. Extrinsic time delays such as device geometries and traps will affect the detector response time in much the same way as the bulk detector. The transit time of excess carriers in the quantum well will be improved because of improved electronic transport properties such as the absence of ionized impurity scattering centers, better confinement of the photo-excited carriers, and faster hole transit time in lattice-strained quantum wells [43]. Because the bias voltage across the detector is usually high to reduce the transit time and the detector output conductance, high field transport dynamics in

the two-dimensional system such as the real-space transfer will be important in determining the absorption and generation of photo-carriers [44]. More measurements with femto-second optical probing technique will help us to understand these mechanisms.

6.3.4. Effect of NDR on the Voltage Gain

Because of the *k*–space transfer mechanism or the real-space transfer mechanism, I-V curves of certain types of detectors will exhibit negative differential resistance (NDR). As pointed out in previous chapters, an oscillation will take place once the magnitude of negative differential conductance is large enough to overcome the positive conductance (i.e. losses) in the external resonant circuit. Since most of application circuits are stabilized amplifiers, it is interesting to find out how the NDR will influence the voltage gain of a detector.

A two-terminal detector can be modeled as the equivalent circuit shown in Fig. 6.3 with a photo-current generator I, an output resistance R, external loading (i.e. R_L and C_L) and other parasitics (C_s, L_s, and R_s). Then the low-frequency or DC output power ratio between a negative output resistance ($R=-R_1$) and a positive output resistance ($R=+R_2$) can easily be derived as:

$$\frac{P_1}{P_2}=\left(\frac{R_1}{R_2}\right)^2 \left(\frac{R_L+R_s+R_2}{R_L+R_s-R_1}\right)^2 \tag{6.12}$$

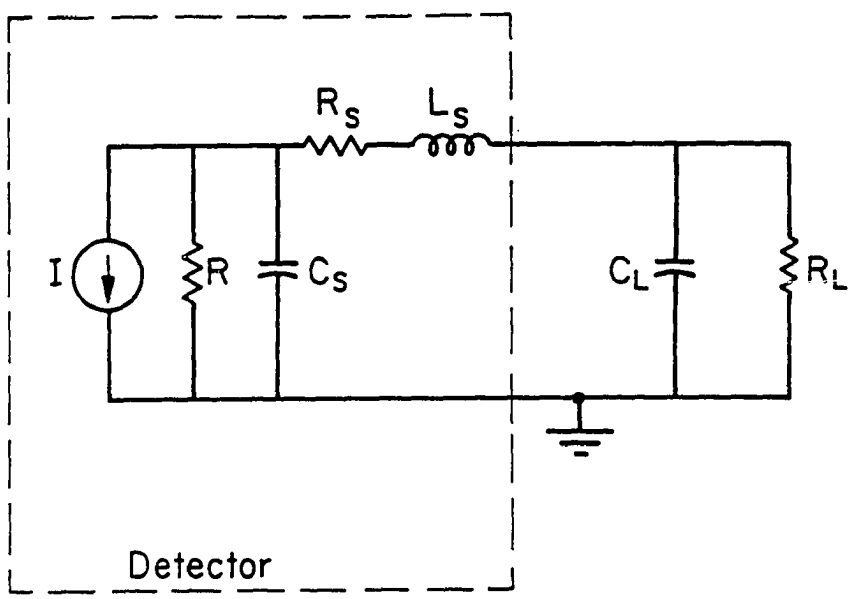

Figure 6.3. Equivalent circuit of a photoconductive detector.

Layer Structure (#OPT–A)

400 Å	n^+ GaAs Cap: $3x10^{18}$ cm^{-3} Si
385 Å	$Al_{0.2}Ga_{0.8}As$: $3x10^{18}$ cm^{-3} Si
20 Å	undoped $Al_{0.2}Ga_{0.8}As$ spacer
150 Å	undoped $In_xGa_{1-x}As$ channel (x from 0.25 to 0.15)
10,000 Å	undoped GaAs buffer
	S.I. GaAs Substrate

Figure 6.4. Layer structure of a single heterojunction MODFET structure with a large amount of interfacial defects (#OPT-A).

$$= \frac{(1+\frac{R_L+R_s}{R_2})^2}{(1-\frac{R_L+R_s}{R_1})^2}$$

It can be seen that the power gain can be greatly increased, if the device exhibits a negative output conductance.

6.4. Experimental data

In this section, optical responses of MODPCD's fabricated on three different modulation-doped structures will be presented. Microwave characteristics of MODFET's fabricated on the same wafer are also examined in order to investigate the influence of different layer structures on the monolithic integration of electronic and optical devices.

6.4.1. Layer structure

Three MBE-grown wafers, including one single-side doped pseudomorphic MODFET structure (layer #OPT-A) and two pseudomorphic double heterojunction MODFET (DH-MODFET) structure (layer #OPT-B and #OPT-C), were fabricated and characterized. The layer structures of layer #OPT-A is depicted in Fig. 6.4. The layer #OPT-B utilizes the same DH-MODFET structure in Chapter 4 with a superlattice buffer, while layer OPT-C is the same one with a buried p^+-GaAs buffer layer. To illustrate the importance of the quality of the buffer and substrate layers, a very high defect density was created at the channel-buffer interface of layer #OPT-A by a large amount of mismatch dislocations.

These dislocations are the results of the excessive indium mole fraction at the channel/buffer interface, which exceeds the maximum amount of the lattice strain to be absorbed elastically by the lattice [45]. As the result of the high defect density, both the electrical and optical performances are degraded, and will be reported in Section 6.4.2.

As reported in Chap. 4, microwave performances of MODFET's can be significantly enhanced by using a high barrier buffer layer. The thick superlattice buffer layer in OPT-B improves the quality of the channel layer, and very fast optical response are reported in Section 6.4.3. Although the high frequency gain of MODFET's can be improved with a buried p^+-GaAs buffer layer, added hole traps in the buried p-type buffer layer increase the gain of the MODPCD detectors at the expense of speed. The optical performance of MODPCD's on OPT-C will be discussed in Section 6.4.4.

6.4.2. Defects in the Epitaxial Layer

The DC drain I-V characteristics of a 1 x 100 $(\mu m)^2$ MODFET fabricated on layer #OPT-A is shown in Fig. 6.5a. Its very soft pinch-off characteristics signals the existence of undesirable buffer/substrate current underneath the active channel. Even a fairly high transconductance (g_m) can be achieved in Fig. 6.5b, the second g_m peak near pinch-off indicates a low-performance parasitic conduction channel. As the result, a very poor current-gain cut-off frequency (f_T) of 8 GHz was obtained from the measured s-parameters.

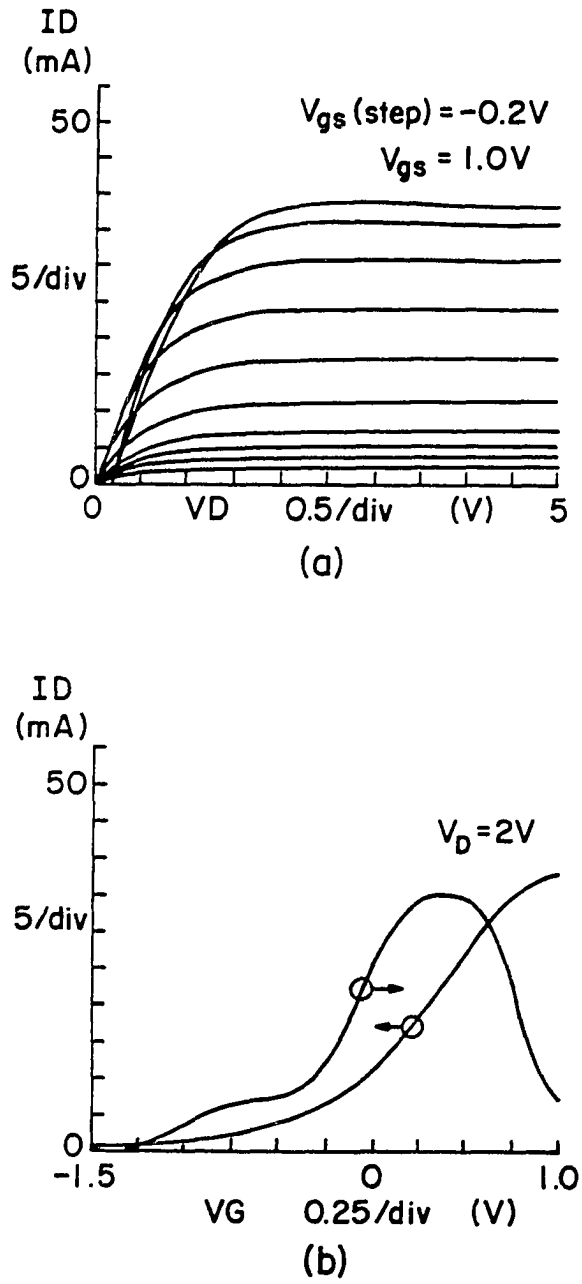

Figure 6.5. (a) DC I-V characteristics of a 1X100 $(\mu m)^2$ MODFET on #OPT-A. (b) g_m versus V_{GS} plot.

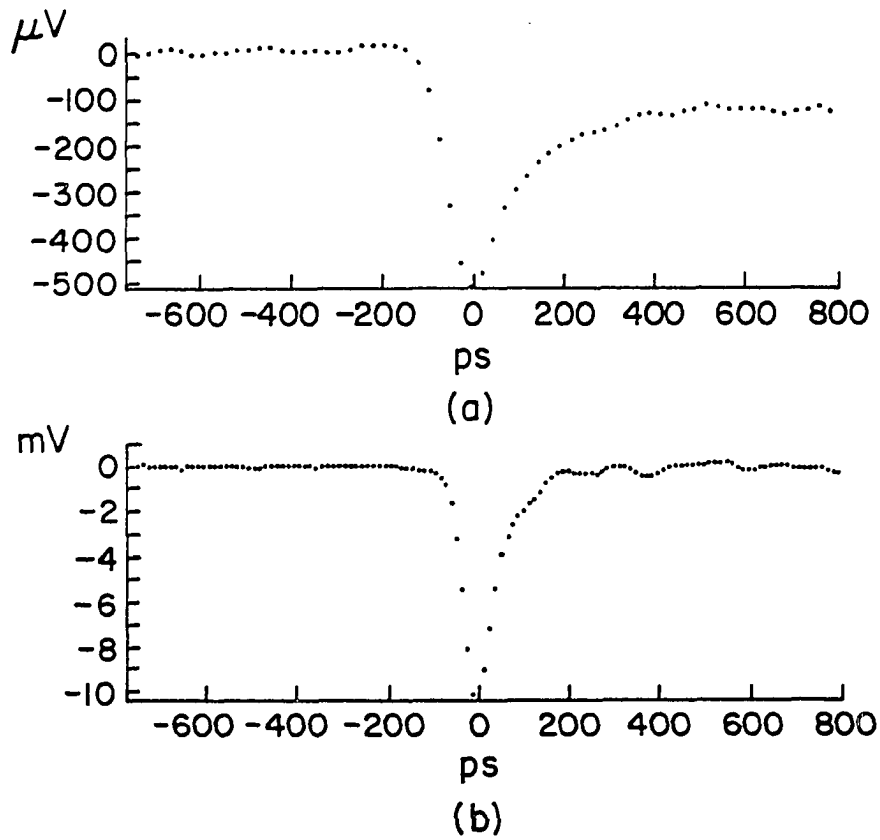

Figure 6.6. (a) Measured time response of MODPCD from layer #OPT-A.
(b) Measured time response of the reference PIN diode.

The optical response of the MODPCD from the same wafer is shown in Fig. 6.6a together with the response of the reference ORTEL's PIN detector in Fig. 6.6b. The wavelength of the light source is 800nm with a FWHM pulse width of 32ps. The measured optical response of the MOPCD is 200 ps at its FWHM, and a long tail with a 1.6 ns time constant can also be observed compared to the reference ORTEL's PIN detector in Fig. 6.6b. The traps created by the mismatch defects in the buffer layer increases the effective lifetime of the excess carriers and then the optical gain. This leads to a very high signal gain at low frequency ($< 1/2\pi\tau_n$), but it results in a very narrow 3 dB bandwidth of 105 MHz in the frequency domain after using the Fast Fourier Transformation (FFT). Therefore, defects and traps in the buffer layer will degrade the high frequency performance of both MODPCDs and MODFETs.

6.4.3. Superlattice-Buffer MODPCD

As discussed in Chap. 4, the superlattice buffer layer is very effective in reducing the defects and impurities segregated from the substrate. It also serve as an energy barrier to confine the 2DEG. The $Al_{0.3}Ga_{0.7}As$/GaAs superlattice buffer layer with an effective bandgap about 1.8eV [46] is transparent to the incoming 800nm (1.5eV) radiation and will not generate excess electron-hole pairs. The 0.5-μm thick superlattice buffer layer also serves as an energy barrier to block the photo-generated carriers in the GaAs substrate from contributing a photocurrent to the electrodes on the surface. In the absence of contribu-

tions of substrate photoexcited carriers which usually have longer lifetime from surrounding traps and defects, the performance of the detector is then determined by the high-quality quantum well channel.

This layer structure is identical to the one utilized to study the bias-dependent microwave characteristics of DH-MODFETs in Chapter 3. Monolithically integrated MODFET's of 1-μm gate length show a room temperature peak extrinsic DC transconductance (g_m) of 400 mS/mm with a full channel current of 610 mA/mm. For 0.3-μm MODFET's, an extrinsic DC g_m of 505 mS/mm and a full channel current of 720 mA/mm are obtained. The high quality quantum well channel also yields a high current-gain cut-off frequency (f_T) of 22 GHz.

Fig. 6.7a shows the picosecond time-domain response of a MODPCD from wafer OPT-B under 800nm 32ps laser pulses. A response time of 50 ps (FWHM) is achieved with an optical gain of 0.3. The frequency response is plotted in Fig. 6.7b by performing FFT on the measured time domain response. It shows a broad 3dB bandwidth up to 10 GHz can be obtained. The low optical gain is the result of the thin 200A light-sensitive quantum well, which can be improved by using modulation-doped multiple quantum wells structures [47].

After applying the deconvolution technique to remove the 32 ps finite pulse width of laser light, an impulse response time of 38.4 ps, including the device and circuit loading parasitics, can be obtained. It is very difficult to estimate how much RC time delay is contributed by 50-Ω interconnection cables and the input

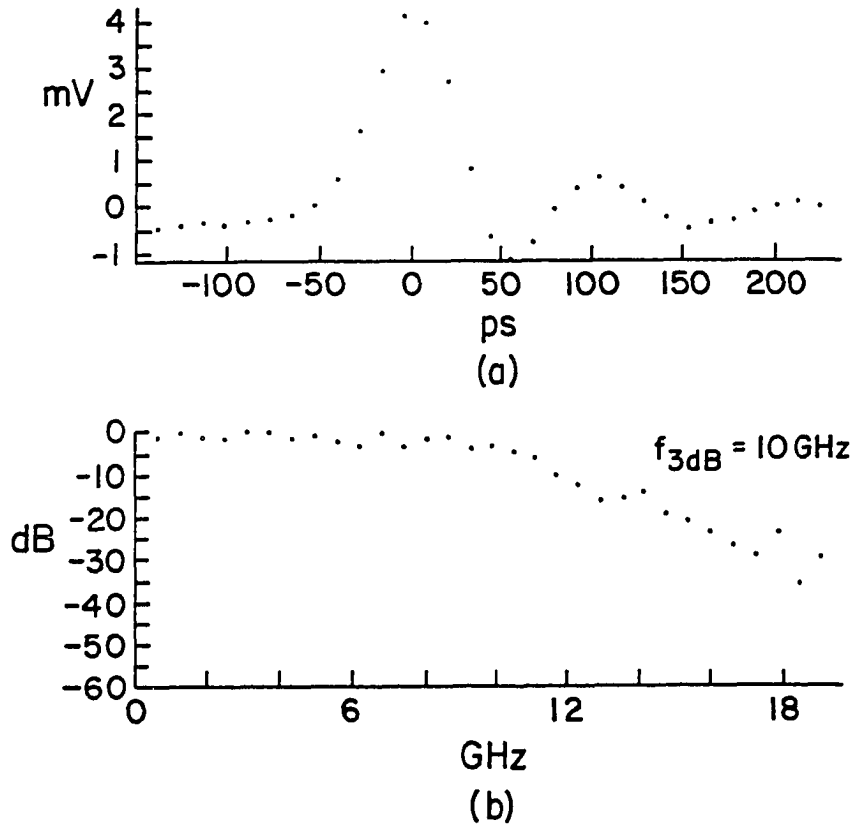

Figure 6.7. (a) Picosecond response of a MODPCD with a superlattice buffer layer. (b) Frequency domain response of (a).

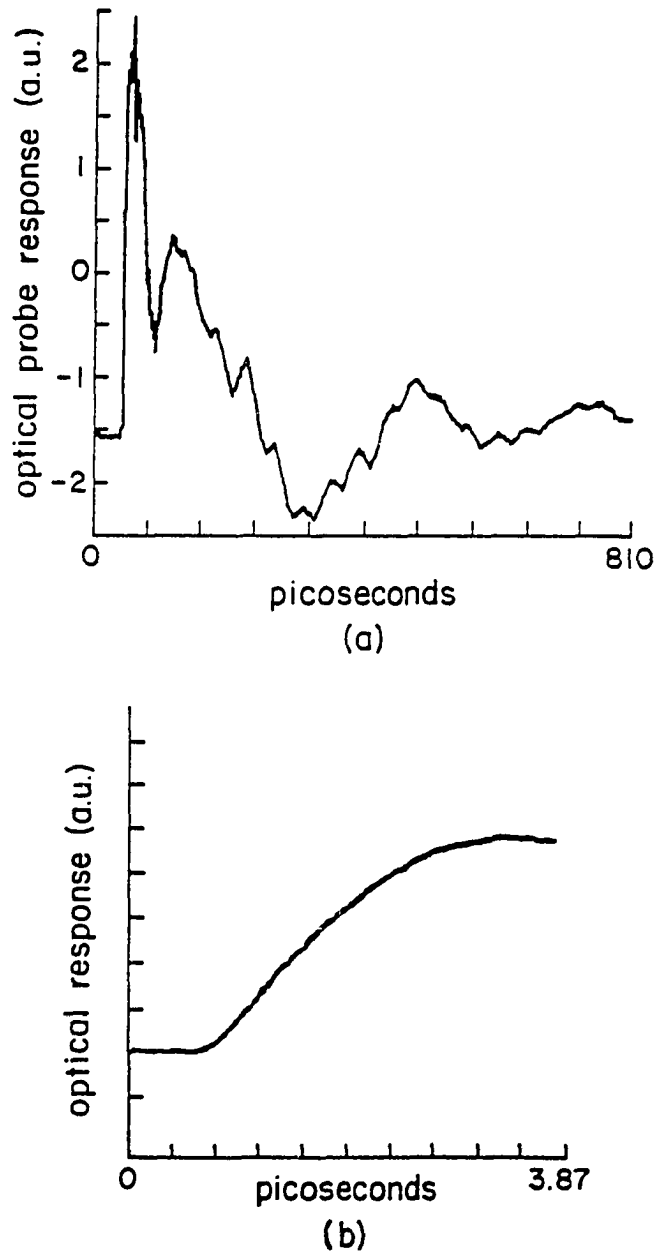

Figure 3.6. Time response of a MODPCD with a superlattice buffer layer (#OPT-B) under 610 nm 100 fs light pulses.

RC delay of the sampling head. However, the RC time constant from the output parasitics can be estimated from the equivalent circuit model in Fig. 6.4. A FWHM RC time delay of 28 ps (0.7RC) can be calculated with a R_L of 50-Ω and a C_{ds} of 800 *fF* determined from microwave measurements. The total response time of the detector is the convolution of the incident light pulse with all of the time delays such as the intrinsic absorption/relaxation processes, RC time delay from internal device parasitics, and delays imposed by external circuit elements as expressed by Eq. 6.8. In this case, a response time of 30ps to an impulse light source can be calculated by assuming a 2ps time response from absorption/relaxation processes, a 28 ps RC delay from the detector parasitics, and a 5ps RC time constant from the external circuits.

The picosecond response of another MODPCD from wafer OPT-B is shown in Fig. 6.8 under 610 nm 100 fs (FWHM) light pulses. The output signal is picked-up with an optical probing technique directly from the electrical field on a bonding wire of the detector. This femtosecond optical measurement, performed at University of Rochester, is measuring the optical impulse response of the intrinsic absorption/relaxation processes and the RC time delay of the detector output parasitics. This differs from those femtosecond probe techniques discussed in previous sections which study the initial absorption/relaxation mechanisms of the hot carrier plasma by monitoring changes of optical properties of semiconductors by reflection or transmission.

Despite multiple reflections from discontinuities of impedance in the fixture, a pulse width (FWHM) of 35 ps together with a risetime of 2 ps is obtained. Because the incident light pulse is very short, the pulse response using this measurement technique actually represents the combined delays of the absorption/relaxation processes and the RC delays of the intrinsic device parasitics. This delay is very close to the estimated delay time of 30 ps calculated in the past paragraph using the output parasitics from an integrated MODFET. Nevertheless, these results indicate that RC parasitics of the detector dominate the impulse response of this MODPCD under very short light pulses (e.g. pulse width of the light is less than the transit time of the excess carriers).

6.4.4. p^+-GaAs-Buffer MODPCD

The energy barrier provided by the buried p^+-GaAs buffer has been found to be very effective in isolating the active FET channel from the impurities and defects in the substrate and in reducing the short channel effects through better carrier confinement as described in Chap. 4. It is understood that the enhanced high frequency gain of the buried p-buffer DH-MODFETs fabricated on wafer OPT-C comes from better carrier confinements rather than improved transport properties in the channel. Actually, out-diffused beryllium acceptor atoms from the p-type buffer degrade the f_T of the fabricated MODFETs. In order to reduce the beryllium out-diffusion, a thick (1000A) undoped set-back layer has been introduced between the p-type doping spike and the silicon doping spike in the

bottom electron supplying layer. MODFETs with a 1.2-μm gate length demonstrate a high extrinsic g_m of 382 mS/mm and a good f_{MAG} at room temperature despite a degraded f_T of 16.5 GHz. The high frequency gain is further improved to 14 dB at 26.5 GHz for a MODFET with a 0.3-μm gate length as the result of excellent carrier confinement.

This may be an optimal modulation-doped heterostructure for FET applications. However, the added hole traps and the potential notch for holes at the p-type doping spike may increase the effective excess carrier lifetime and deteriorate the high-speed response of the integrated MODPCD. The importance of removing the low-speed minority holes in the buffer layer of a MODPCD to improve the gain-bandwidth product was first demonstrated by Chen, et al. [48] with a p-type back gate contact. The detector's fall time in Chen's experiment was reduced from 1 ns to 450 ps down to 80 ps. The noise power of the detector was also reduced by applying the back gate bias. However, the buried p^+-GaAs buffer layer is totally depleted in the high frequency FET applications in order to reduce the parasitic capacitance from the backside p-type channel. In this section, the results of MODPCD's with a floated p-type back gate is reported.

Fig. 6.9 shows the detector response to a 800nm 32ps (FWHM) light pulse on a sampling oscilloscope. This MODPCD is fabricated on wafer OPT-C with a totally depleted buried p^+-GaAs buffer layer. A 250ps pulse width was meas-

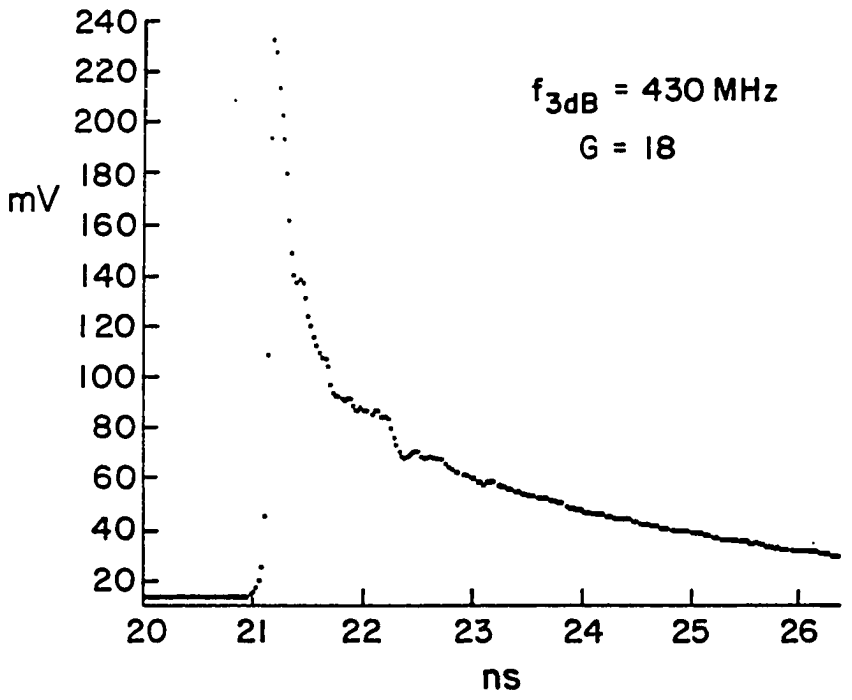

Figure 6.9. Time response of a MODPCD with a buried p^+-GaAs buffer layer (#OPT-C) under 820 nm picosecond light pulses.

ured at FWHM together with a 2.3ns long exponential decaying tail. After processed by fast Fourier transformation, a 3dB bandwidth of 400 MHz was obtained. Because of the long minority carrier lifetime, the optical gain is increased significantly to 1,800%, obtained from the reference PIN diode with a gain of 85%. Although the unequalized detector may appear to be too slow to serve high speed optical detections, it can still be utilized for high sensitive receivers at moderate transmission speed of a few hundred megahertz. It may still be able to detect gigabit optical signal with its large gain-bandwidth product, if an external high-pass equalizer is used to lower the sensitivity and to broaden the bandwidth.

6.5. Summary

In this chapter, optical responses of interdigitated photoconductive detectors using various modulation-doped heterostructures are characterized with picosecond light pulses. Because the large optical penetration depth of 800nm light source in GaAs, the speed and gain of the optical detector is greatly influenced by the material quality and layer configuration of the buffer layer. Different optimization parameters in the buffer layers are identified by comparing the optical responses of MODPCDs and the microwave characteristics of MODFETs integrated on the same wafer. Defects and traps in the buffer or substrate deteriorate the high frequency performance of both MODPCD and MODFET. While the buried p-type buffer enhances the high frequency gain of the

MODFET with better carrier confinement, traps in the buffer layer increase the lifetime of the minority holes. The long lifetime of excess carriers increases the optical gain but at the expense of degraded performance in speed and bandwidth.

The best buffer layer configuration to fabricate high speed MODPCDs and high frequency MODFETs monolithically is employing a thick superlattice with an effective bandgap above the incident photon energy. The superlattice buffer is very effective in gettering the out-diffused impurities from the substrate and to provide a high energy barrier to spatially separate carriers between the channel and substrate. High speed response of MODFETs and MODPCDs are obtained with the better transport properties in the purer epitaxial layers grown on superlattice buffers. The high barrier superlattice buffer layer generates more microwave gain through better carrier confinement and prevents the slow photoexcited carriers in the substrate from contributing to the photocurrent to the external circuits.

From the measured data, an intrinsic detector response time of 30ps (FWHM) can be derived with either picosecond or femtosecond light sources. A fast risetime of 2ps is also obtained. This response time is largely determined by the output RC parasitics of the detector which need further optimization.

Multiple modulation-doped quantum well structures in combination with a thick superlattice buffer layer should be investigated to increase the optical gain

of MODPCD as well as the current density of MODFETs needed for high speed digital circuits.

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CHAPTER 7

DUAL-GATE MODFETS

7.1. Introduction

GaAs dual-gate MESFETs play very important roles in various high performance microwave circuits such as variable gain control stages for both low noise and power amplifiers [1], active phase shifters [2], and mixers [3]. The advantage of the dual-gate structure comes from the added functionalities by integrating two independent FETs in a compact manner. Compared to the single-gate FET, the dual-gate FET of the same gate length provides the same input impedance with higher output impedance, higher RF power gain, and much reduced feedback parasitics [4-6].

Single gate MODFETs have demonstrated excellent microwave performance with lower noise, and higher cut-off frequency than GaAs MESFETs [7]. However, the dual-gate MODFET has not been studied before for microwave circuit applications. In this chapter, the fabrication and characterization of dual-gate MODFETs with either 1.2-μm or 0.3-μm gate length will be reported. Their DC and microwave performances are also compared to single-gate MODFETs fabricated on the same wafer. This is the first successful fabrication of dual-gate MODFETs. Dual-gate MODFETs demonstrate stable and higher available gain than single-gate MODFETs over a broad frequency up to f_T. The small-signal

equivalent circuit will be analyzed to study different microwave gain roll-of characteristics.

7.2. Layer Structure and Device Fabrication

The pseudomorphic double heterojunction structure is grown by MBE on top of a semi-insulating LEC substrate in the following sequence: 5000 A of superlattice buffer layer, 50 A undoped GaAs, silicon doping plane with a density of 2 x 10^{12} cm^{-2}, 85 A undoped GaAs, 200 A undoped InGaAs channel, 30 A undoped AlGaAs spacer, silicon doping plane of 6 x 10^{12} cm^{-2}, 250 A undoped AlGaAs, and 400 A GaAs capping layer with a silicon doping density of 1 x 10^{18} cm^{-3}. The mole fractions of aluminum and indium are 30% and 15% respectively. The superlattice buffer in this structure has been found to be very effective in reducing the short channel effects as investigated in Chapter 4.

The grown layers were then fabricated with a conventional recess-gate FET process outlined in Chapter 3: mesa etch, Ni/AuGe/Ag/Au ohmic contact alloyed at 450 C for 10 seconds, gate level lithography, recess etch of the capping layer, and Ti/Pd/Au gate metallization. A specific ohmic contact resistance (R_c) of 0.05 ohm-mm was obtained from the transmission line measurements. The gate lithography was performed by using either a mid-UV contact aligner for 1.2-μm gate length or electron beam direct writing for 0.3-μm gate length. A PMMA/P(MMA-MAA)/ PMMA triple layer resist system has been developed to reduce the resistance of submicron gates as described in Chapter 3. Fig. 7.1

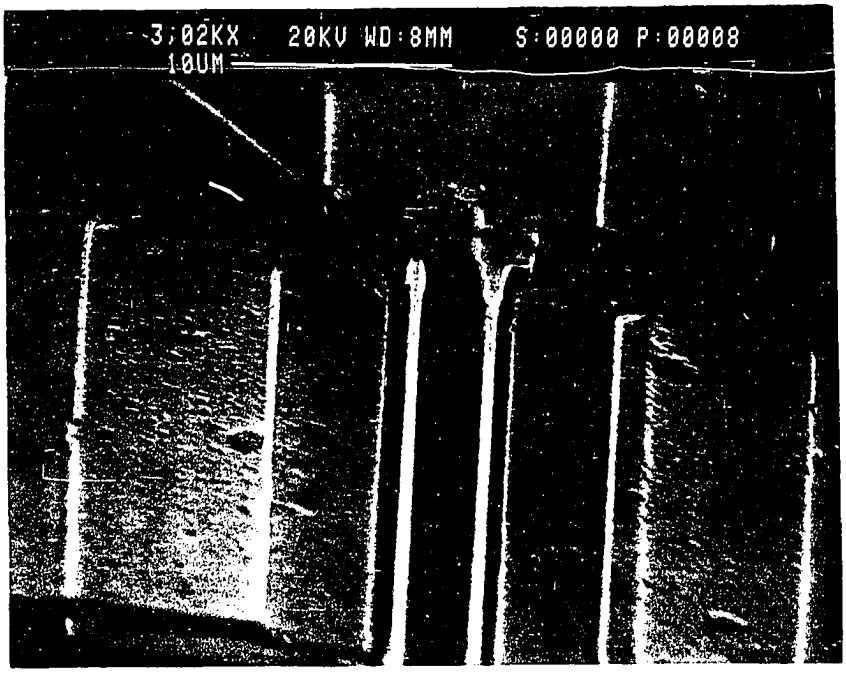

Figure 7.1. SEM microphotograph shows a pair of dual gates with 0.3-μm footprints.

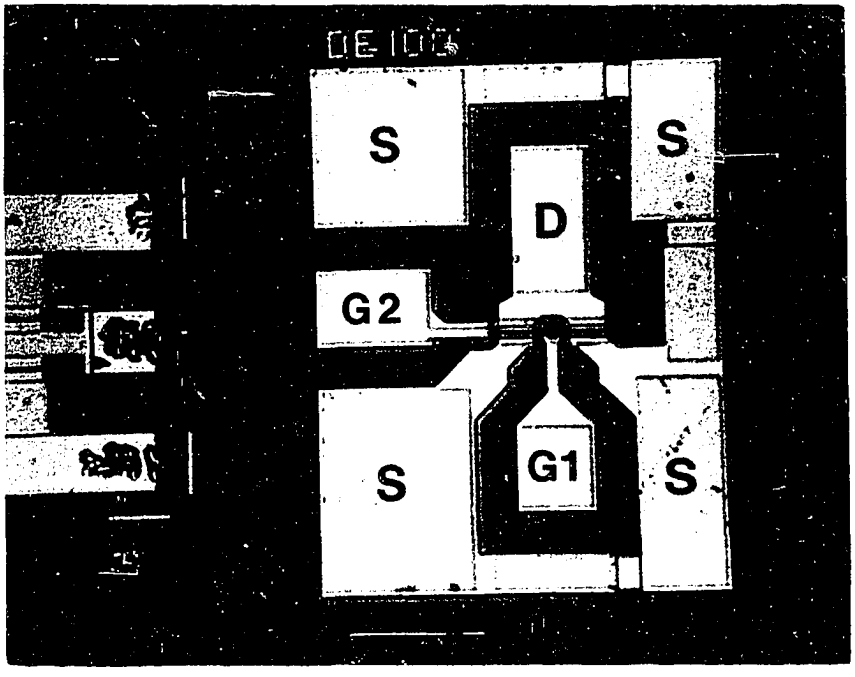

Figure 7.2. Microphotograph shows a fabricated dual-gate MODFET with a layout for microwave probing.

shows the SEM microphotograph of two 0.3-μm gate fingers between the source and drain ohmic contact. The $gate_1$-to-source, $gate_2$-to-drain, and $gate_1$-to-$gate_2$ spacings are 0.75 μm, 0.75 μm, and 2.5 μm respectively. The large separation between two control gates is necessary to reduce the proximity effect in the electron beam lithography. Fig. 7.2 shows a fabricated dual-gate MODFET with a layout suitable for three-port microwave probing.

7.3. DC Characteristics

Fig. 7.3 shows the DC drain I-V characteristics of a 0.3 X 100 μm dual-gate MODFET with the second gate biased at 2 V. It shows a very good DC output conductance, similar to dual-gate MESFETs [5]. When the drain is biased below 1.3 V, the forward conduction current through the second gate causes abnormal behaviors in the I-V characteristics. The dependence of DC transconductance (g_m) and drain current (I_d) on V_{g1} and V_{g2} with the drain biased at 4 volts is shown in Fig. 7.4. The envelope of the g_m curves corresponds to the g_m versus Vg curve of a single-gate MODFET. g_m of the dual gate MODFET increases as the bias of the second gate becomes more positive. g_m can be approximated as

$$g_m = g_{m1}\left(1 - \frac{1}{1 + g_{m2}R_{ds1} + R_{ds1}/R_{ds2}}\right) \qquad (7.1)$$

from the equivalent circuit model in Fig. 7.5 [5], where g_{m1}, g_{m2}, R_{ds1}, and R_{ds2} are the transconductances and output resistances of the FET1 and FET2. From Eq. 7.1, g_m of the dual-gate MODFET is always lower than that of the

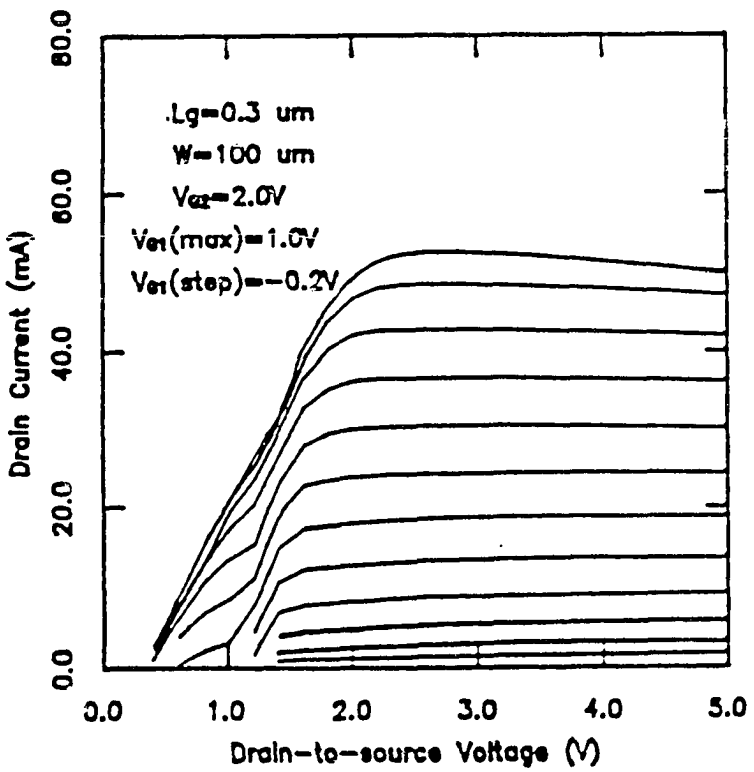

Figure 7.3. DC I-V characteristics of a 0.3 X 100 μm dual-gate MODFET with V_{G2}=+2.0V.

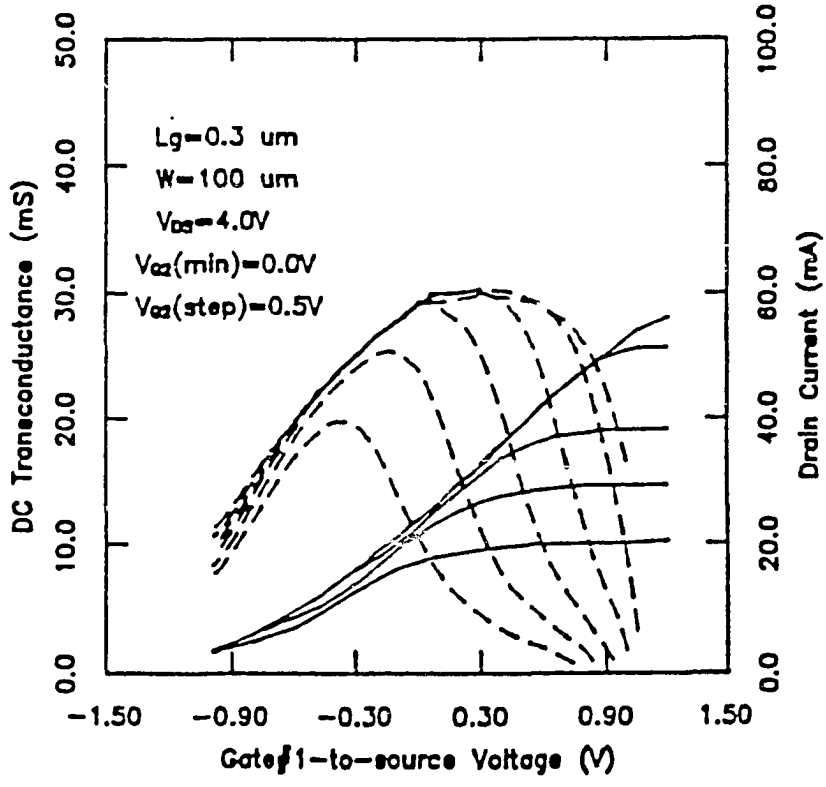

Figure 7.4. g_m and I_D characteristics of a 0.3 x 100 μm dual-gate MODFET under various V_{G1} and V_{G2} with V_{DS}= 4V.

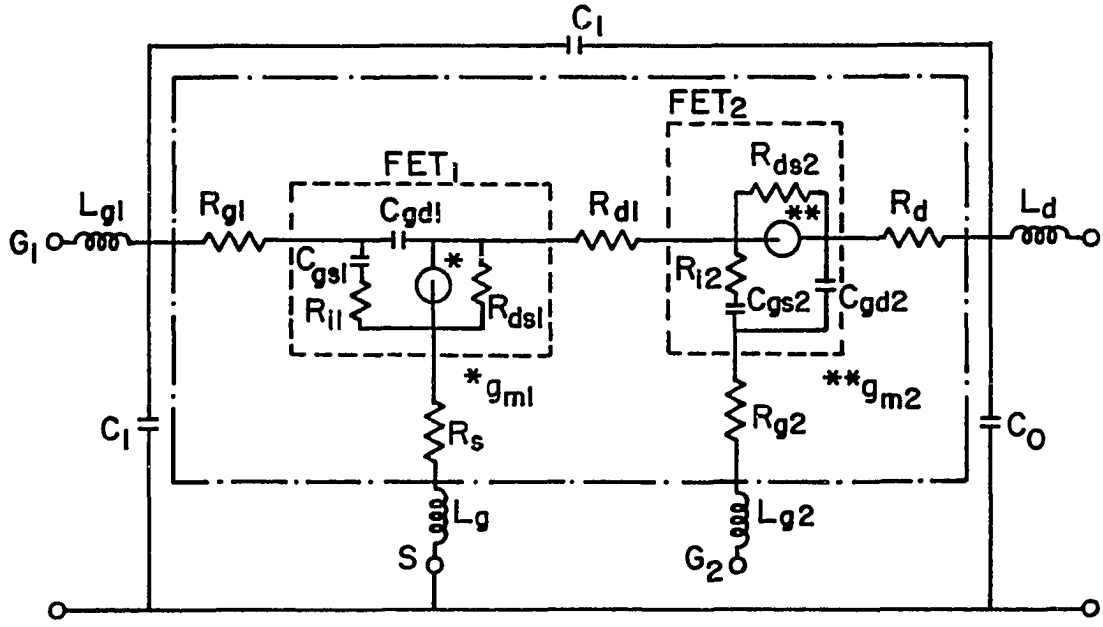

Figure 7.5. Small-signal equivalent circuit of a dual-gate MODFET.

corresponding single-gate MODFET. A peak g_m of 303 mS/mm and a full channel current of 535 mA/mm are obtained from a 0.3 X 100 μm dual-gate MODFET while the single-gate MODFET shows a peak g_m of 500 mS/mm. To obtain a precise current-voltage relation, $I_d(V_{g1},V_{g2},V_{ds})$, a computer program is usually required [5].

7.4. Microwave Performance

The S-parameter measurements were performed from 0.5 GHz to 26.5 GHz with microwave wafer probes. The second gate of dual-gate MODFET is RF-terminated with a 50-ohm load for broad-band two-port characterization. This avoids the potential instability of the device over the whole measuring frequency range.

7.4.1. S-Parameters

Measured S-parameters from dual-gate MODFETs with 1.2-μm and 0.3-μm gate length are plotted in Fig. 7.6 and Fig. 7.7 respectively together. S-parameters taken from single-gate MODFETs on the same wafer are also plotted for comparisons. It shows almost identical S_{11} curves, because the input impedance is dominated by the first gate. The magnitude of the S_{12} curve of dual-gate MODFETs is reduced dramatically from those of single-gate MODFETs because of good isolation between input and output by the second gate. The magnitude of S_{21} curves of dual-gate MODFETs is higher because of

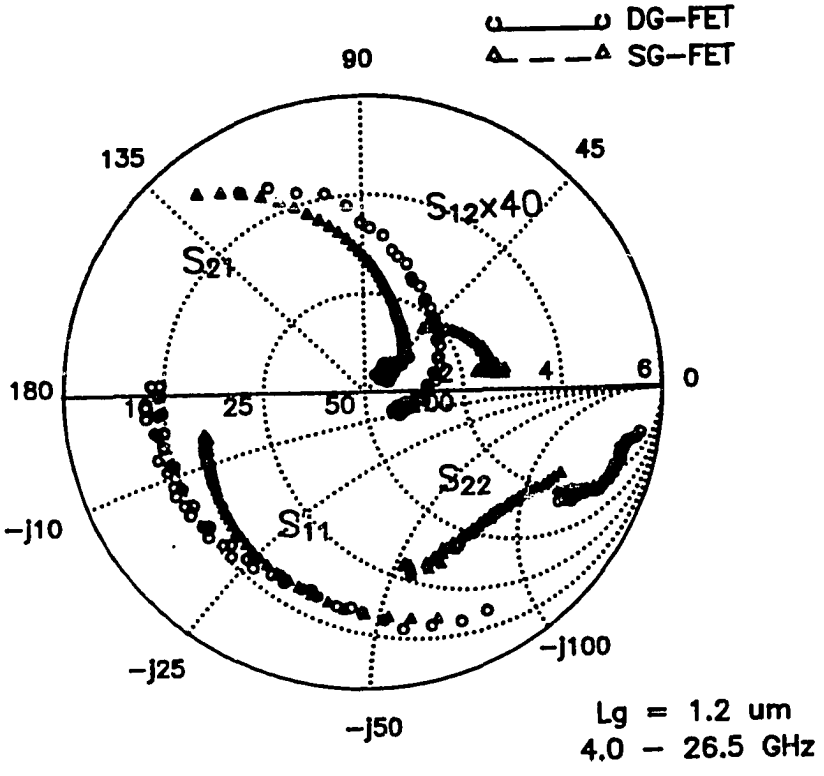

Figure 7.6. Measured S-parameters of single-gate and dual-gate MODFETs with 1.2-μm gate length.

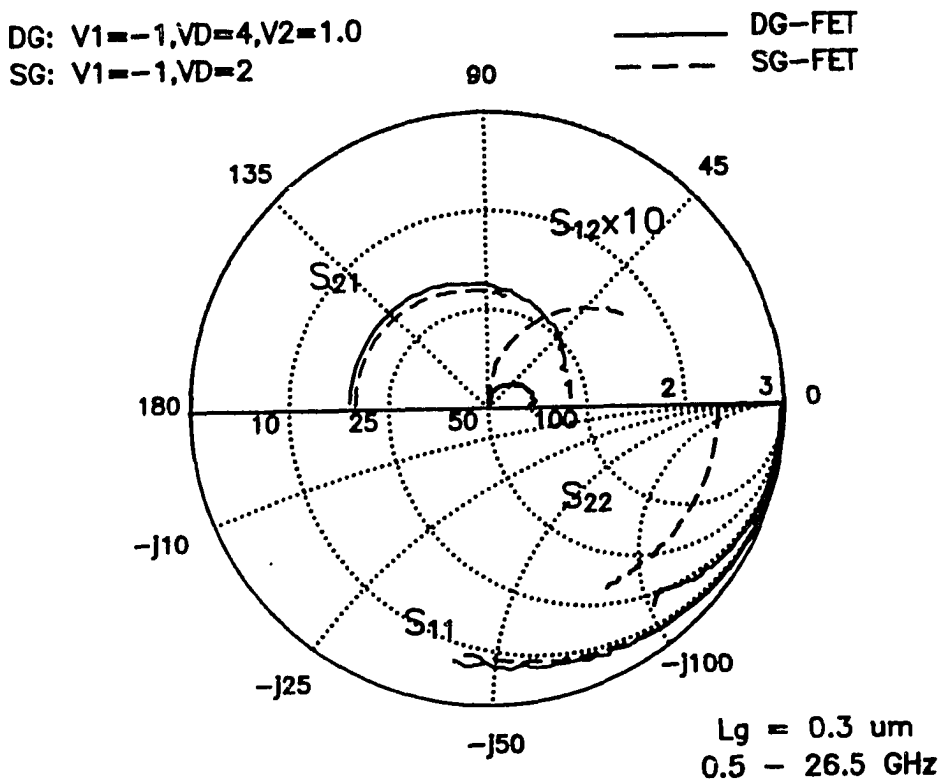

Figure 7.7. Measured S-parameters of single-gate and dual-gate MODFETs with 0.3-μm gate length.

improved overall output impedance. Greater phase shift of S_{21} is introduced by the extra delay from the second FET. Improved output impedance causes the S_{22} of dual-gate MODFET to shift toward the infinite resistance circle of the Smith Chart. The output resistance of a dual-gate MODFET at low frequency can be derived as

$$R_{ds} = R_{ds1} + R_{ds2} + g_{m2}R_{ds1}R_{ds2} . \tag{7.2}$$

It indicates that very high output impedance and high voltage gain can be obtained with the dual-gate configuration.

7.4.2. Cut-Off Frequencies

Maximum Stable Gain (MSG), Maximum Available Gain (MAG), and short-circuit current gain (h_{21}) are calculated from S-parameters and are depicted in Fig. 7.8 for both single-gate and dual-gate MODFETs with 1.2-μm gate length. Current gain cut-off frequency (f_T) as high as 21.5 GHz and an MAG cut-off frequency (f_{MAG}) of 57 GHz can be extrapolated from the 1.2-μm single-gate MODFET. At frequencies below 5 GHz, the stability factor (k) of the dual-gate MODFET is less than unity and its MSG is higher than that of the single-gate MODFET. Both MSG's are decreasing with a -3 dB/octave slope. Beyond 5 GHz, the dual-gate MODFET is unconditionally stable, the MAG is decreasing with a -6 dB/octave slope till 12 GHz. The MAG gain slope switches to -12 dB/octave for frequencies higher than 12 GHz. For the single-gate MODFET, the MAG decreases with a -6 dB/ocatve slope above 9 GHz with a k-factor

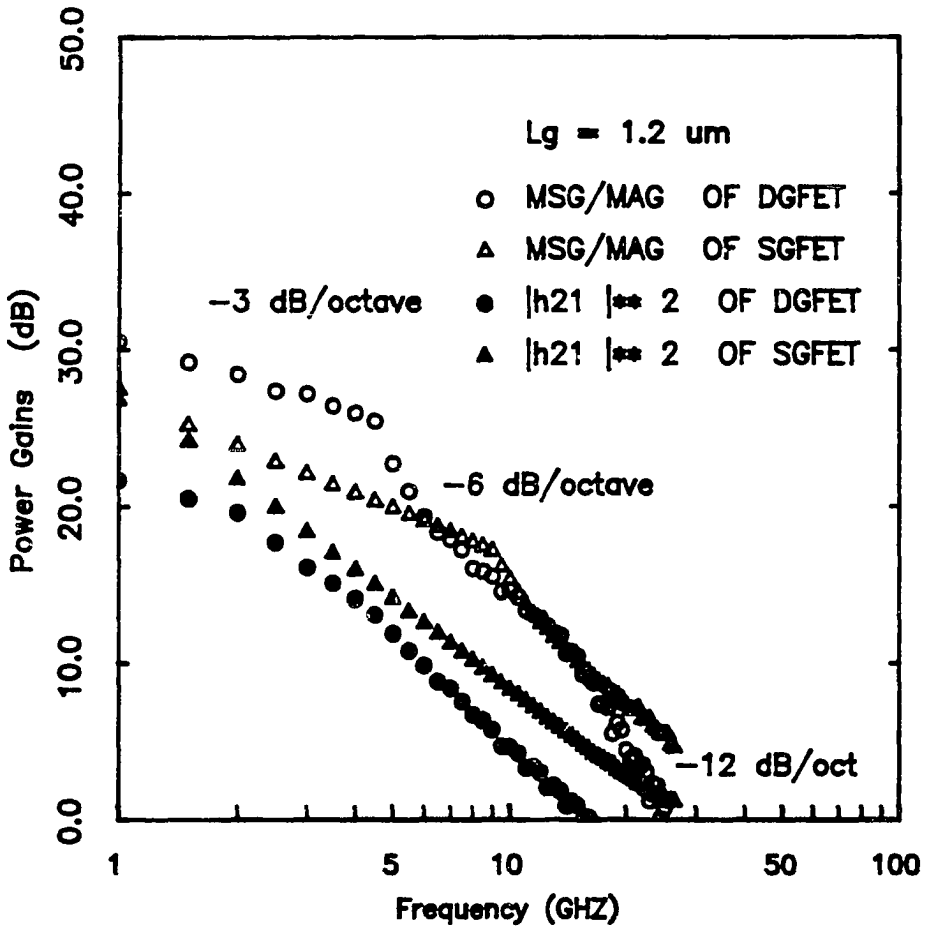

Figure 7.8. Power gain vs. frequency for single-gate and dual-gate MODFETs with 1.2-μm gate length.

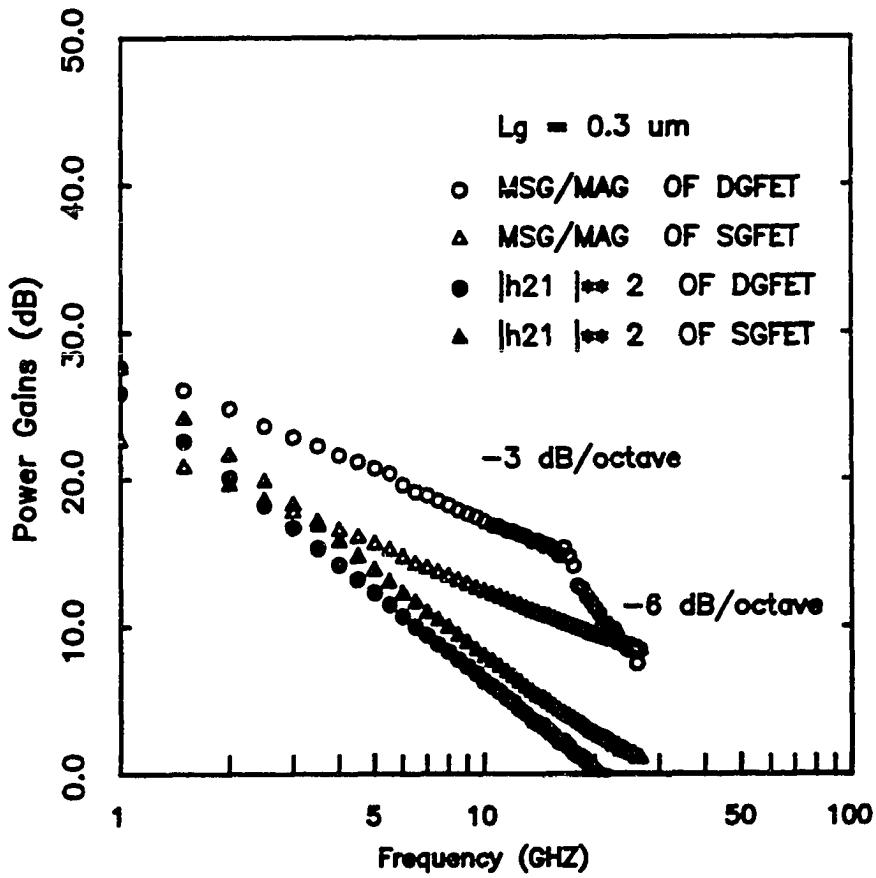

Figure 7.9. Power gain vs. frequency for single-gate and dual-gate MODFETs with 0.3-μm gate length.

greater than one. It is fair to say that, the dual-gate MODFET is more stable and generating higher gain than the single-gate MODFET over a broad frequency range from 5 GHz to 19 GHz. This feature makes dual-gate MODFETs very useful for the applications from low frequency up to f_T.

The dual-gate MODFET with 0.3-μm gate length exhibits a similar frequency dependence on power gains as shown in Fig. 7.9. Because of the improved device performance and reduced parasitics in short channel devices, the corner frequency with unity k factor is displaced to a higher frequency. Consequently, the -12 dB/octave slope cannot be observed over the measurement bandwidth. Since both f_T and f_{MAG} depend on the gate and drain biases, a peak f_T of 57 GHz and an MSG of 14 dB with k factor equal to 0.6 at 26 GHz were obtained from the 0.3-μm single gate MODFET under other bias conditions. An f_{MAG} of 180 GHz can then be extrapolated with a -6 dB/octave slope.

7.4.3. Small-Signal Equivalent Circuit Model

The frequency-dependent gain-slope of dual-gate MODFETs can be explained with the equivalent circuit model in Fig. 7.5. The dual-gate MODFET is modeled as two individual single-gate MODFETs in cascade. After some arithmetics and manipulation of the equivalent circuit, the microwave figures-of-merit of the single-gate and dual-gate MODFETs can be calculated. For single-gate MODFETs, a -3dB/octave MSG gain slope can be found as

$$MSG_{SG} \approx \frac{g_m}{2\pi f} , \tag{7.3}$$

with the stability factor almost a linear function of frequency:

$$k_{SG} \approx \frac{f}{f_T} \frac{\left[\frac{2f_p}{f_i} + \frac{f_T}{f_i}\right]}{\left[1 + j\,\frac{f}{f_i}\right]} , \tag{7.4}$$

where

$$f_T = \frac{g_m}{2\pi C_{gs}} , \tag{7.5}$$

$$f_i = \frac{1}{2\pi C_{gs}(R_i + R_g + R_s)} , \text{ and} \tag{7.6}$$

$$f_p = \frac{1}{2\pi C_{gd} R_{ds}} . \tag{7.7}$$

When k is greater than one, the maximum available gain of the single-gate MODFET is

$$MAG_{SG} = \frac{\left[\frac{f_T}{f}\right]^2}{2(R_g + R_i + R_s)\left(\frac{2}{R_{ds}} + 2\pi f_T C_{gd}\right)} . \tag{7.8}$$

The stable gain MAG_{SG} is rolling-off with a -6 dB/octave slope with the frequency.

For the dual-gate MODFETs, the maximum stable gain MSG_{DG} is

$$MSG_{DG} = MSG_1 \; MSG_2 \tag{7.9}$$

$$\approx \frac{g_{m1}}{2\pi f C_{gd1}} \frac{g_{m2}}{g_{d2}} ,$$

with a stability factor of

$$k_{DG} \approx K_1 + \frac{2f}{f_{T2}} \quad . \tag{7.10}$$

If k_{DG} is greater than one, the maximum available gain of a dual-gate MODFET is then

$$MAG_{DG} \approx \left[\frac{f_{T1}\, f_{T2}}{f^2}\right] \frac{f(k_{DG})}{|Z_{g1}| \left[f\left[C_f\left(1-j\,\frac{f_{T2}}{f}\right)+\frac{C_{gd2}}{R_{ds2}}\right] + 2\pi f^2 C_{ds2} C_{gd2}\right]} \tag{7.11}$$

where

$$Z_{g1} = (R_{g1}+R_{i1}+R_s) + \frac{(1+R_s g_{m1})}{j\,2\pi f C_{gs1}} \quad , \tag{7.12}$$

and $f(k_{DG})$ is a weak function of k_{DG}.

It can be seen that the stability factor (k_{DG}) of a dual-gate MODFET increases in a faster rate with the frequency than the one for the single-gate MODFET. Therefore, the dual-gate MODFET becomes unconditionally stable at lower frequency. From Eq. 7.12, the stable gain MAG_{DG} is first decreasing with -6dB/octave in the first term at low frequency band, and then decreases with -12dB/octave at higher frequency dominated by both denominators.

7.5. Summary

Dual-gate MODFETs of either 1.2-μm or 0.3-μm gate length have been successfully fabricated and characterized for the first time. Observed power gain slopes for dual-gate MODFETs are -3 dB/octave for MSG at low fre-

quency, -6 dB/octave for MAG at intermediate frequency, and -12 dB/octave at high frequency. Dual gate MODFETs are more stable and provide higher gain than single-gate MODFETs over most of the operating frequency range. Dual-gate MODFETs are very promising for millimeter-wave circuit applications such as gain control blocks, mixers and active phase-shifters.

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CHAPTER 8

CONCLUSIONS

8.1. Summary

The scope of this thesis is to investigate the high frequency limit of the multiple heterojunction MODFET for large signal applications.

The gate charge control of planar-doped MODFETs is investigated theoretically as a prerequisite to studying their high frequency performance limits. Non-linear behaviors of a DH-MODFET under large-signal operations are studied with experimentally determined bias-dependent equivalent circuit models. Distinctive features of MODFETs such as heterojunction charge transfer, AlGaAs parallel conduction, quantum-well confinement, and real-space transfer are found to be very important in optimizing the high frequency performance.

The idea of using a high barrier buffer layer, such as the buried superlattice or the buried p^+-GaAs layer, to enhance the charge control of the inverted heterointerface of a DH-MODFET is first introduced by this work. From the study of these buffer layer structures, it is found that high barrier buffers reduce the carrier deconfinement and the substrate conduction to improve the device gain at high frequencies. The buried p^+-GaAs is more effective in confining the hot 2DEG and improving the f_{MAG} in the short channel devices, while the super-

lattice buffer improves both the f_T and the channel current through a higher quality 2DEG channel. As the result of this study, f_{MAG}'s of DH-MODFETs with high barrier layers are as high as the state-of-the-art single heterojunction MODFETs but with much higher current and power densities.

The negative differential drain resistance is also first reported in the MODFET structure with very fast RF characteristics. By analyzing the characteristics of MODFETs in the NDR region, the existence of real-space transfer of hot 2DEG over the heterointerface is identified. The short transit-time of the NDR in this study should be very promising for microwave and millimeter-wave generation.

Dual-gate MODFETs and photoconductive detectors are also fabricated on DH-MODFET structures to demonstrate potential applications in high-speed electronic and opto-electronic integrated circuits. The limitations of these device are studied and compared to the experimental data.

8.2. Suggestions for Future Work

The charge control model is not completed without being implemented on a circuit simulator such as SPICE. Further developments on the model to incorporate other dynamics such as hot electron induced buffer and gate current are necessary to predict the device characteristics accurately. The AC bias-dependent model should also be incorporated.

Although the buried p-GaAs buffer is very effective to reduce the buffer current, it would be desirable to develop a doped p-superlattice buffer for both higher f_T and higher f_{MAG}. The real-space transfer mechanism is a very interesting and important device dynamics which will limit the performance of MODFETs, and should be investigated further. The effective confinement of hot 2DEG electrons in a MODFET structure can also be achieved with high-barrier spacer and buffer layers.

With the advancement of MBE and MOVPE technologies, MODFETs have successfully been implemented on other material systems grown on a lattice-matched substrate such as in AlInAs/GaInAs/InP [1] and InP/GaInAs/InP [2] with very good performance. Hetero-epitaxial growth of MODFET structures on lattice-mismatched substrates, such as GaAs on Si [3] and $Al_{0.5}In_{0.5}As/Ga_{0.5}Ga_{0.5}As$ on GaAs [4], have been demonstrated recently with a great potential for the next generation high speed semiconductor technology. The material quality of the epitaxial layer is usually affected by the defects and impurities in the buffer and substrate. It would be very desirable to apply the high-barrier buffer technique developed in this work on these new material systems to enhance the device performance and to isolate defects from the active channel.

8.3. References

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